KAWA ELECTRONIC RESEARCH & DEVELOPMENT CENTRE

Service Manual

Reference No. : **SM- GPDP421DAIA1LS-002**
Revision : **0**
Date : **2007.June.**
Page : **P.1 of 150**

In House Model No. : **PDP421D**
Customer Model No. : **PDP42Z5TAC**

BOM No : **GPDP 421DAIA1LS–B02**

Description : **Service Manual for PDP42Z5TAC_LG X3A_CANADA**

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Received By: **MK Department** [illegible]

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0	Initial Release	2007-6-21

AKAI

SERVICE MANUAL

Model: PDP42Z5TAC

This manual is the latest at the time of printing, and does not Include the modification which may be made after the printing, By the constant improvement of product.

Safety Precaution

CAUTION

RISK OF ELECTRIC SHOCK
DO NOT OPEN

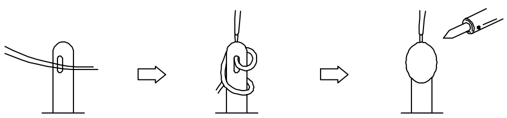
CAUTION: TO REDUCE THE RISK OF ELECTRIC SHOCK, DO NOT REMOVE COVER (OR BACK). NO USER-SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED SERVICE PERSONNEL ONLY.

The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of uninsulated “dangerous voltage” within the product’s enclo sure that may be of sufficient magnitude to constitute a risk of electric shock to persons.

The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.

PRECAUTIONS DURING SERVICING

1. In addition to safety, other parts and assemblies are specified for conformance with such regulations as those applying to spurious radiation. These must also be replaced only with specified replacements.
   Examples: RF converters, tuner units, antenna selection switches, RF cables, noise-blocking capacitors, noise-blocking filters, etc.
2. Use specified internal Wiring. Note especially:
   1) Wires covered with PVC tubing
   2) Double insulated wires
   3) High voltage leads
3. Use specified insulating materials for hazardous live parts. Note especially:
   1) Insulating Tape
   2) PVC tubing
   3) Spacers (insulating barriers)
   4) Insulating sheets for transistors
   5) Plastic screws for fixing micro switches
4. When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.), wrap ends of wires securely about the terminals before soldering.



5. Make sure that wires do not contact heat generating parts (heat sinks, oxide metal film resistors, fusible resistors, etc.)
6. Check if replaced wires do not contact sharply edged or pointed parts.
7. Make sure that foreign objects (screws, solder droplets, etc.) do not remain inside the set.

MAKE YOUR CONTRIBUTION TO PROTECT THE ENVIRONMENT

Used batteries with the ISO symbol for recycling as well as small accumulators (rechargeable batteries), mini-batteries (cells) and starter batteries should not be thrown into the garbage can.

Please leave them at an appropriate depot.

WARNING:

Before servicing this TV receiver, read the SAFETY INSTRUCTION and PRODUCT SAFETY NOTICE.

SAFETY INSTRUCTION

The service should not be attempted by anyone unfamiliar with the necessary instructions on this apparatus. The following are the necessary instructions to be observed before servicing.

1. An isolation transformer should be connected in the power line between the receiver and the AC line when a service is performed on the primary of the converter transformer of the set.
2. Comply with all caution and safety related provided on the back of the cabinet, inside the cabinet, on the chassis or picture tube.
3. To avoid a shock hazard, always discharge the picture tube's anode to the chassis ground before removing the anode cap.
4. Completely discharge the high potential voltage of the picture tube before handling. The picture tube is a vacuum and if broken, the glass will explode.

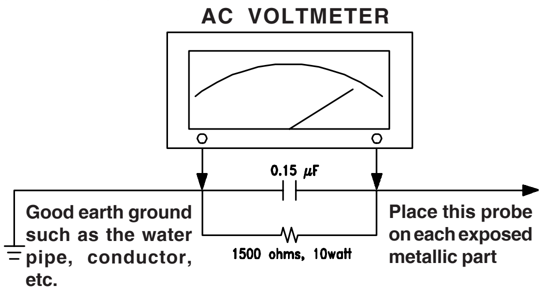
5. When replacing a MAIN PCB in the cabinet, always be certain that all protective are installed properly such as control knobs, adjustment covers or shields, barriers, isolation resistor networks etc.
6. When servicing is required, observe the original lead dressing. Extra precaution should be given to assure correct lead dressing in the high voltage area.
7. Keep wires away from high voltage or high tempera ture components.
8. Before returning the set to the customer, always perform an AC leakage current check on the exposed metallic parts of the cabinet, such as antennas, terminals, screwheads,metal overlay, control shafts, etc., to be sure the set is safe to operate without danger of electrical shock. Plug the AC line cord directly to the AC outlet (do not use a line isolation transformer during this check). Use an AC voltmeter having 5K ohms volt sensitivity or more in the following manner.

   Connect a 1.5K ohm 10 watt resistor paralleled by a 0.15μF AC type capacitor, between a good earth ground (water pipe, conductor etc.,) and the exposed metallic parts, one at a time. Measure the AC voltage across the combination of the 1.5K ohm resistor and 0.15 uF capacitor. Reverse the AC plug at the AC outlet and repeat the AC voltage measurements for each exposed metallic part.

   The measured voltage must not exceed 0.3V RMS.

   This corresponds to 0.5mA AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.

   The resistance measurement should be done between accessible exposed metal parts and power cord plug prongs with the power switch "ON". The resistance should be more than 6M ohms.



AC Leakage Current Check

PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in this apparatus have special safety-related characteristics.

These characteristics are offer passed unnoticed by visual spection and the protection afforded by them cannot necessarily be obtained by using replacement components rates for a higher voltage, wattage, etc.

The replacement parts which have these special safety characteristics are identified by ⚠ marks on the schematic diagram and on the parts list.

Before replacing any of these components, read the parts list in this manual carefully. The use of substitute replacement parts which do not have the same safety characteristics as specified in the parts list may create shock, fire, or other hazards.

9. Must be sure that the ground wire of the AC inlet is connected with the ground of the apparatus properly.

Trouble Shooting Manual of PDP

1 Do not power on

1.1 Please check the AC cable if connect to AC plug.
It is true that the connector doesn't connect to AC plug. Please connect it.

1.2 Please check the AC cable if connect to AC power.
It is true that the AC cable doesn't connect to AC power. Please connect it.

1.3 Please check the power board of fuse if broken.
If the F101 fuse is broken, firstly please pull out the AC cable from AC power. Secondly please check whether the AC L power and the AC N ground have shortened, the multimeter read number is infinite, and the fuse is broken. Then look over power board if the Output whether is normal. Please change the power board.

2 The LED (indicator light) is extinguished

2.1 The LED (indicator light) is green or red; to put the power switch when the indicator light is worked. It is true that the Power DC Output have somewhere short circuit.
Please check the connector J2, J11. If not, please connect the direction whether is wrong, or the main board somewhere of power short circuit.

3 The power is normal worked, but doesn't show screen

3.1 The indicator light worked normal (green light).
Please check the main board of transistor Q2 whether rights, if not, it doesn't have +5V voltage. It is true Q2 Collector haven't +5V, to check Q2 if fail. Or to check Q2 of base if not low (low is working, high doesn't working).
Please refer to the attached sheet a circuit diagram.

4 The remote control doesn't be control.

4.1 To check the batteries of remote control if it runs out of.

4.2 To check the main board of connector J3 of wire connects fastness and the connector if broken.
Please refer to the attached sheet a circuit diagram.

5 The sound doesn't output

5.1 To check the main board +24V voltage of connector J2, it's not +24V voltage. Then to check the power main board +24V.
Please refer to the attached sheet a circuit diagram

6 Picture abnormity

Please change the PDP model panel when the picture displays horizontal or vertical level line or flash spots.

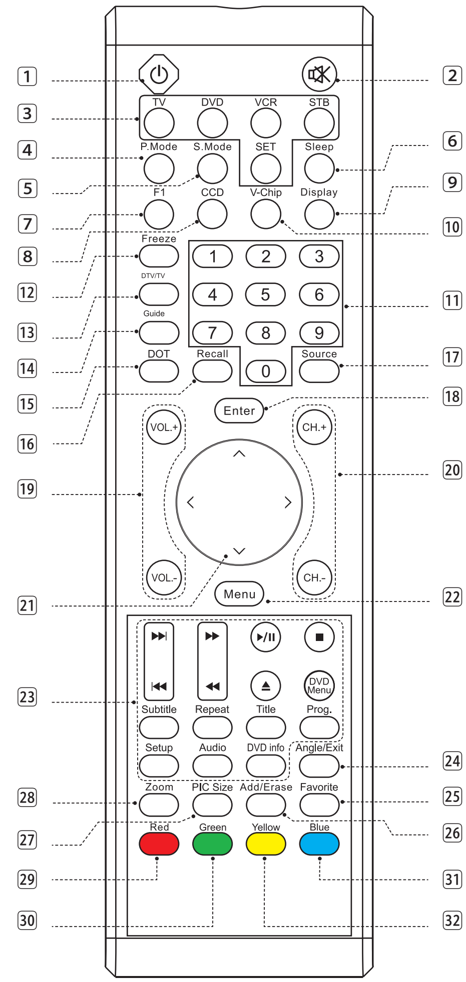
Product Specification

Product Model	PDP42Z5TAC
TV System	NTSC M, ATSC
VIDEO System	NTSC
Screen Size	42” diagonal
Display Area	921.6mm(H) x 519.2mm(V) ± 0.5mm
Aspect Ratio	16:9
External Size (with stand)	1039.8 mm (W) x 757 mm (H) x 275 mm (D)
Net Weight (with stand)	35.5 kg
Display Resolution	1024 (H) x 768 (V) pixels (Each pixel has R/G/B 3 color cells)
Pixel Dot Pitch	0.900 (H) x 0.676 (V) mm
Color	1073.7 millions of colors (R/G/B each 1024 scales)
Gray Scale	1024 (R/G/B each 10-bit)
Brightness (Peak)	1200cd/m^2
Contrast (Peak)	10000:1
Sound Effect	Acoustic Cinema Enhancement
Power Supply	AC 120V, 60 Hz
Power Consumption	350W
Input Terminal	Antenna Input (F Type) x 1 (NTSC + ATSC/Clear QAM)
	HDMI (Ver. 1.2) connector x2
	VGA (D-Sub 15 Pin Type) x 1
	Component Video - YPbPr x 2 RCA Terminals
	Video Input RCA Terminal x 1
	S-Video Input Mini Din 4 Pin Terminal x 1
	Stereo, Audio x 5
Output Terminal	1 set of Audio Output terminals (RCA, L&R)
	SPDIF (Coaxial) x 1

Note: The specifications shown above may be changed without notice for quality improvement.

4.3 Remote Control

(Note: Details refer to AKAI TV Universal Remote Control Programming Guide.)



1 **Standby(⏻):** Press to turn on and off.
2 **Mute(🔇):** Press this button to quiet the sound. Press again to reactivate the sound.
3 Press these buttons to select control of the TV, DVD, VCR or Set-top Box device.
4 **P. Mode**: Press to cycle through picture modes: Cinema, Normal, Vivid, Hi-Bright and User.
5 **S. Mode**: Press to cycle through the sound modes: Normal, News, Cinema, Concert and User.
6 **Sleep**: Press repeatedly until it displays the time in minutes (10, 20, 30, 40, 50, 60, 90, 120 and Off) that you want the TV to remain on before shutting off. To cancel sleep time, press **Sleep** button repeatedly until sleep Off appears.
7 **F1**: Press to cycle through the Stereo and Multi-channel TV sound options: Mono, Stereo and Bilingual.
8 **CCD**: Press to select the Closed Caption mode.
9 **Display**: Press to display the channel information; this information disappears after 9 seconds.
10 **V-Chip**: Select the child protect mode you want.
11 **0~9 Number Buttons**: Press 0~9 to select a channel, and used to input the password; the channel changes after 4 seconds.
12 **Freeze**: Press to freeze the picture, press again to restore the picture.
13 **DTV/TV**: Press to choose DTV/TV (high definition channels) directly.
14 **Guide (Digital TV Timetable)**: Press to display the (Digital TV Timetable) mode. Press again to exit.
15 **DOT:** Press number buttons with it to select the channels directly in DTV.(i.e. channel 108-1 would need the dot button after the 8)
16 **Recall**: Press to return to previous channel.
17 **Source**: Press to select the signal source, such as TV, AV, S-Video, YPbPr 1, YPbPr 2, VGA, HDMI 1 or HDMI 2. If you are selecting inputs from the input menu or displaying the OSD menu , press the **Enter** button to confirm your selection.
18 **Enter**: Press to enter or confirm.
19 **VOL +/-**: Press to adjust the volume.
20 **CH +/-** : Press to select the channel forward or backward.
21 ∧, ∨, <, >: Press ∧, ∨, <, > to move the on-screen cursor.
22 **Menu**: Press to enter into the on-screen setup menu, press again to exit.
23 These buttons have no function.
24 **Exit**: Press this button to exit in the menu.
25 **Favorite**: Press to display the favorite channel list. Press ∧ or ∨ to select the channel then press Enter to confirm.
26 **Add/Erase**: Press to add or delete favorite or dislike channels.
27 **Pic Size**: Press to change the screen size, such as Full, 4:3.(Note: When in VGA mode, it can only select “Full”.)
28 **Zoom:** Press repeatedly to zoom the image.
29 **Red**: This is a special control function for the Digital tuner.
30 **Green**: This is a special control function for the Digital tuner.
31 **Blue**: This is a special control function for the Digital tuner.
32 **Yellow**: This is a special control function for the Digital tuner.

8. Support the Signal Mode

A. VGA Mode

Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
640 x 480	31.50	60.00
800 x 600	35.16	56.25
	37.90	60.32
	48.08	72.19
1024 x 768	48.40	60.00

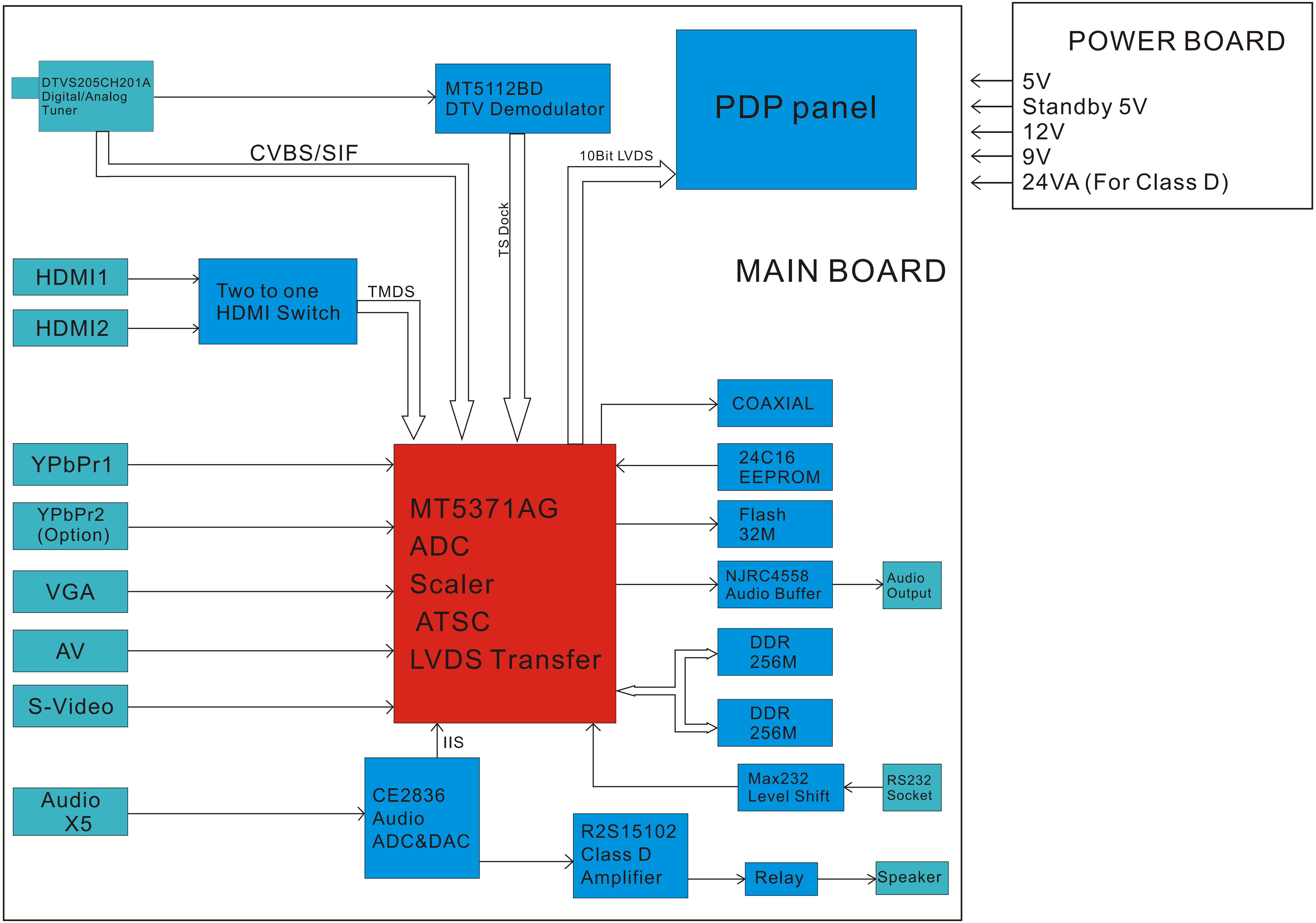
B. YPbPr Mode

Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
480i	15.734	59.94
480p(720x480)	31.468	59.94
720p(1280x720)	45.00	60.00
1080i(1920x1080)	33.75	60.00

C. HDMI Mode

Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
480p	31.468	59.94
720p	45.00	60.00
1080i	33.75	60.00

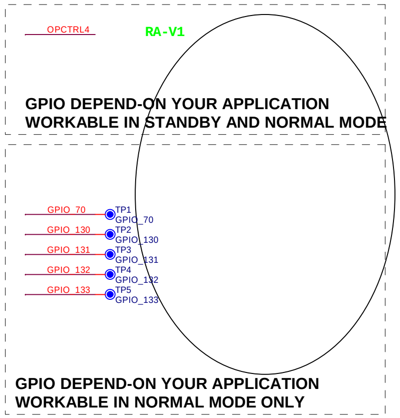
- When the signal received by the Display exceeds the allowed range, a warning message shall appear on the screen.
- You can confirm the input signal format from the on-screen.

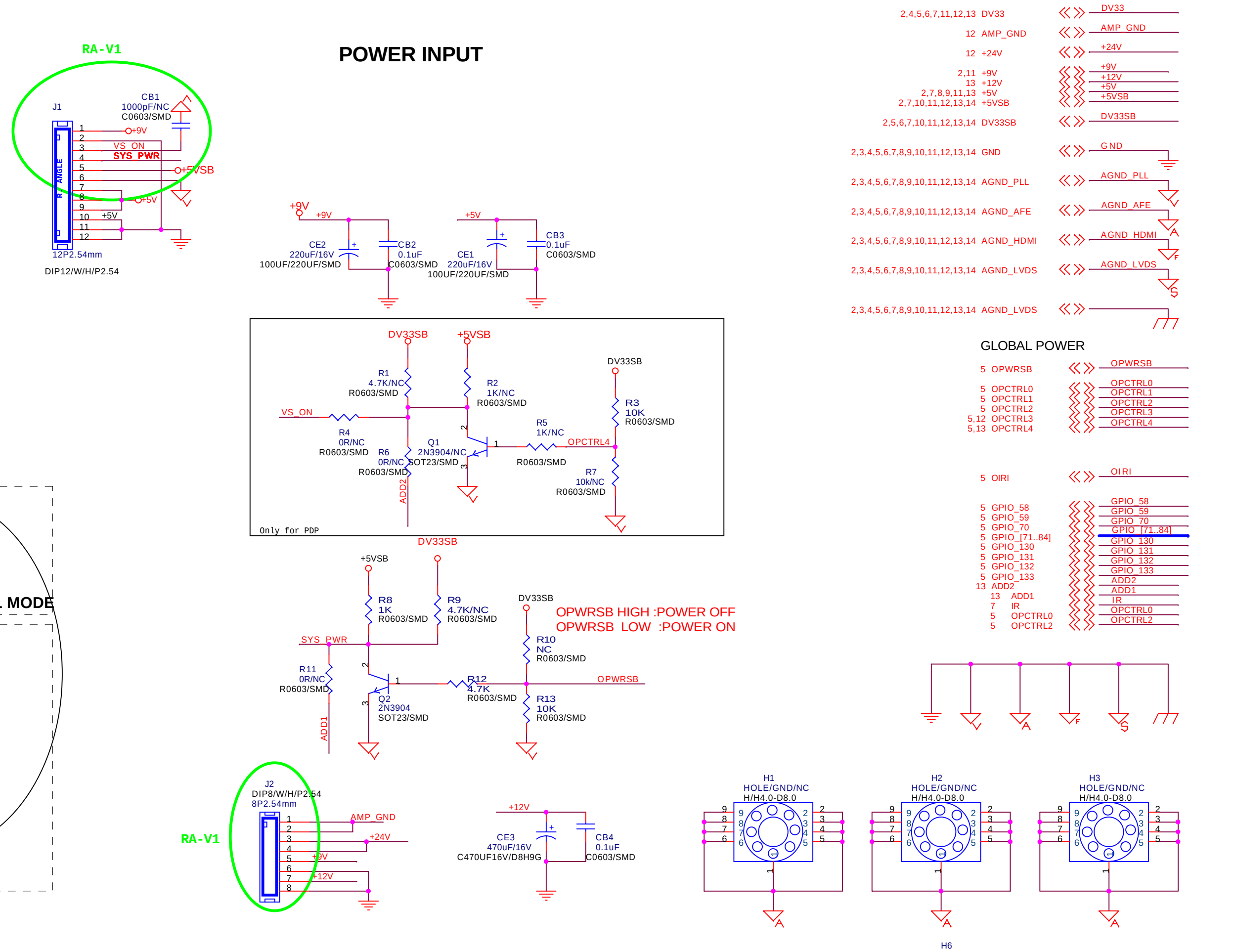

DTVS205CH201A
Digital/Analog
Tuner
MT5112BD
DTV Demodulator
PDP panel
POWER BOARD
5V
Standby 5V
12V
9V
24VA (For Class D)
CVBS/SIF
10Bit LVDS
TS Dock
MAIN BOARD
HDMI1
HDMI2
Two to one
HDMI Switch
TMDS
COAXIAL
YPbPr1
24C16
EEPROM
MT5371AG
ADC
Scaler
ATSC
LVDS Transfer
YPbPr2
(Option)
Flash
32M
VGA
NJRC4558
Audio Buffer
Audio
Output
AV
DDR
256M
S-Video
DDR
256M
IIS
Max232
Level Shift
RS232
Socket
Audio
X5
CE2836
Audio
ADC&DAC
R2S15102
Class D
Amplifier
Relay
Speaker

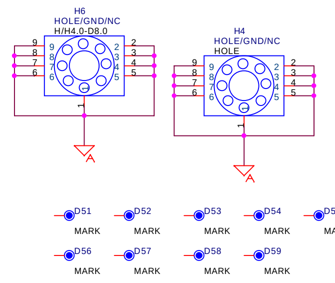
MT5372RAV6

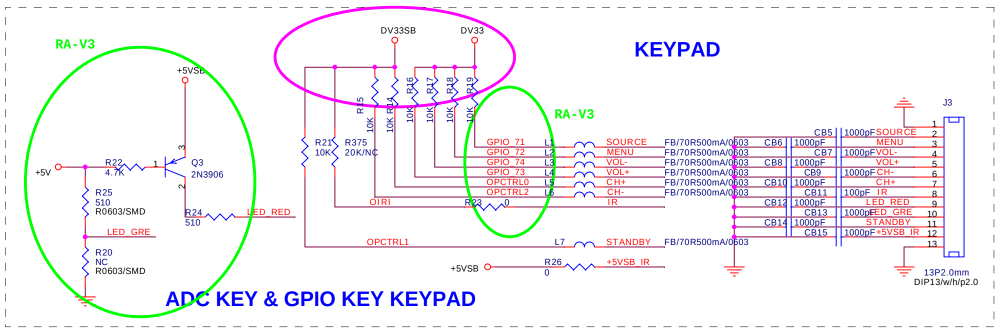
MT5372 (PBGA) REFERENCE DESIGN - 4 LAYERS

Rev	History	DATE
RA-V0	INITIAL VERSION	2006/07/14
RA-V1		2006/07/31
RA-V2		





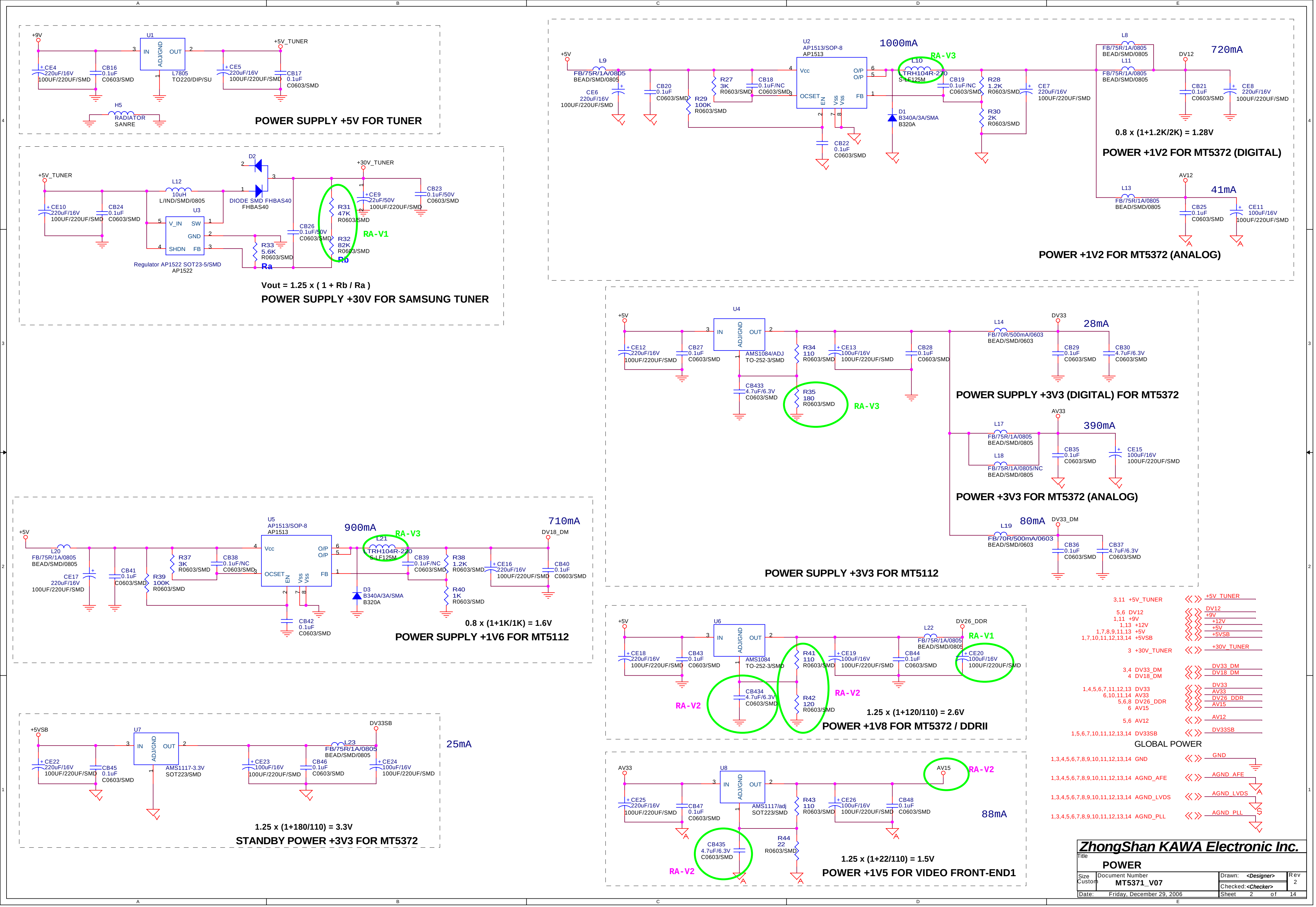


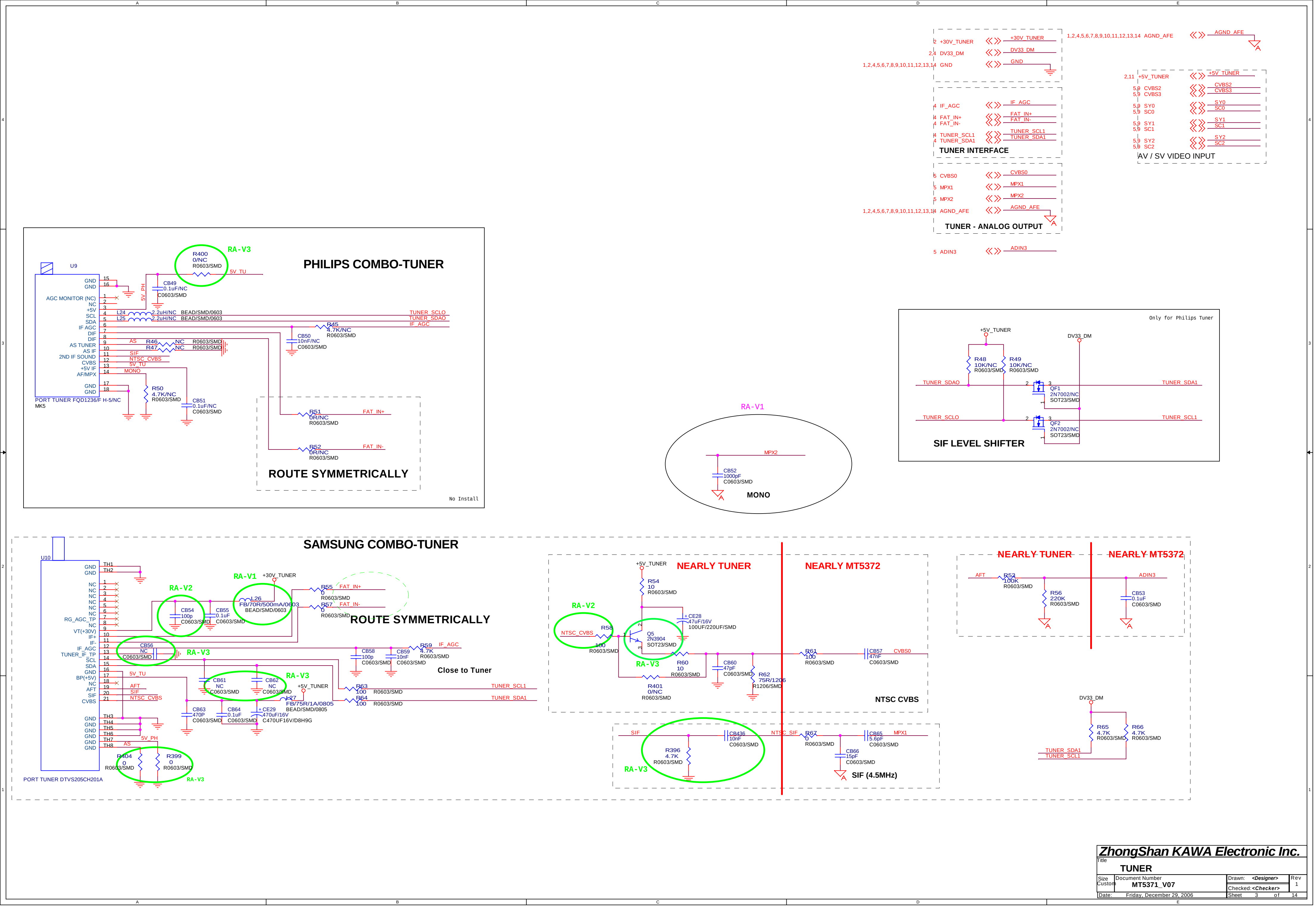


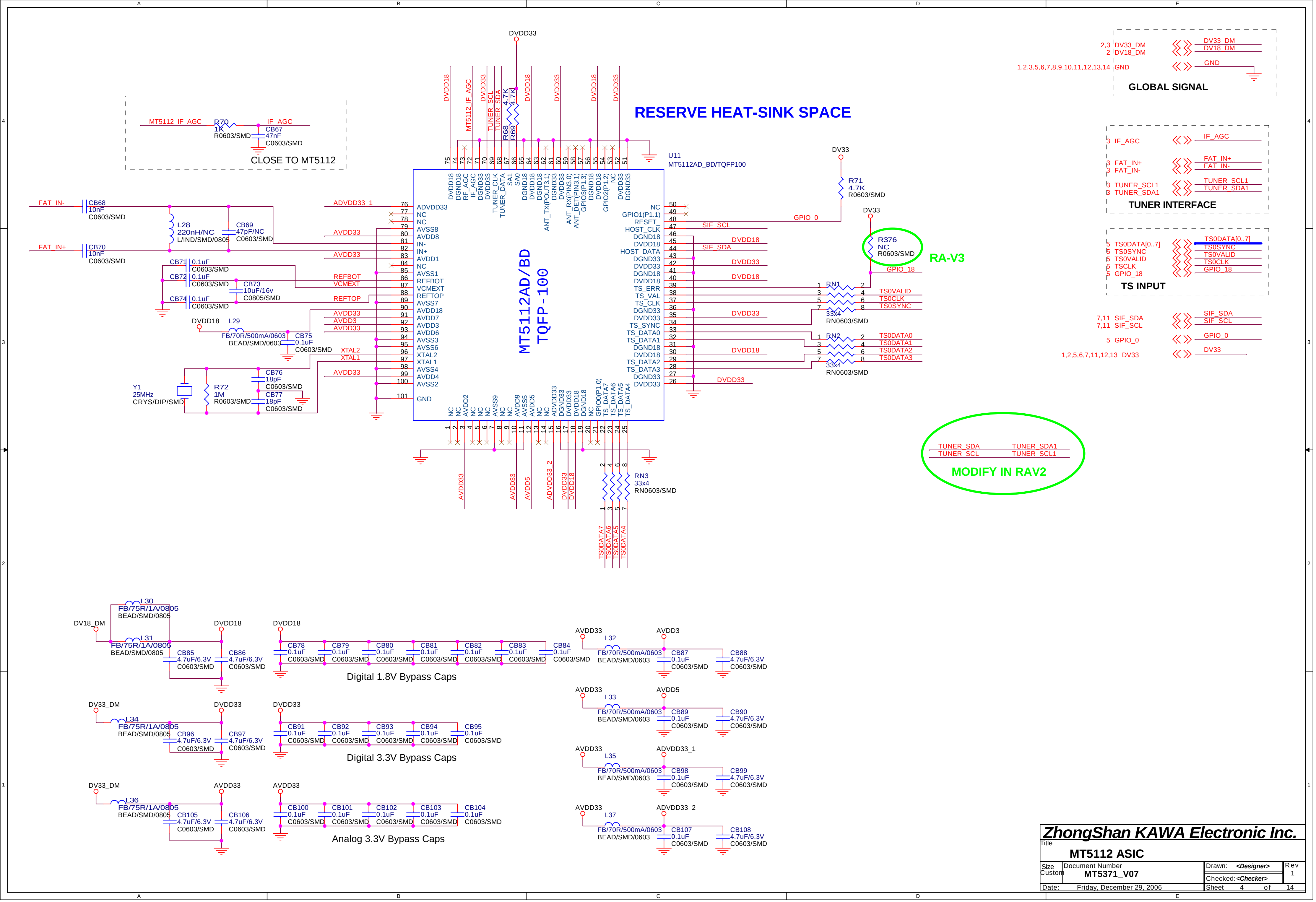
NAME	TYPE	DEVICE
+24V	POWER +24V	POWER SUPPLY
+12V	POWER +12V	POWER SUPPLY
+5V	POWER +5V	POWER SUPPLY
+5VSB	POWER +5V	POWER SUPPLY
DV33SB	POWER +3.3V	STANDBY POWER
+5V_TUENR	POWER +5V	TUNER POWER
DV33_DM	POWER +3.3V	MT5112 POWER AND ITS PERIPHERAL
DV18_DM	POWER +1.6V	MT5112 POWER
DV33	POWER +3.3V	MT5372 POWER AND ITS PERIPHERAL
AV33	POWER +3.3V	MT5372 ANALOG POWER
DV18_DDR	POWER +1.8V	MT5372 DDR POWER
AV15	POWER +1.5V	MT5372 VIDEO FRONT-END POWER
DV12	POWER +1.2V	MT5372 POWER
AV12	POWER +1.2V	MT5372 ANALOG POWER
GND	GROUND	DIGITAL GROUND
AGND_PLL	GROUND	ANALOG GROUND
AGND_AFE	GROUND	ANALOG GROUND
AGND_HDMI	GROUND	ANALOG GROUND
AGND_LVDS	GROUND	ANALOG GROUND

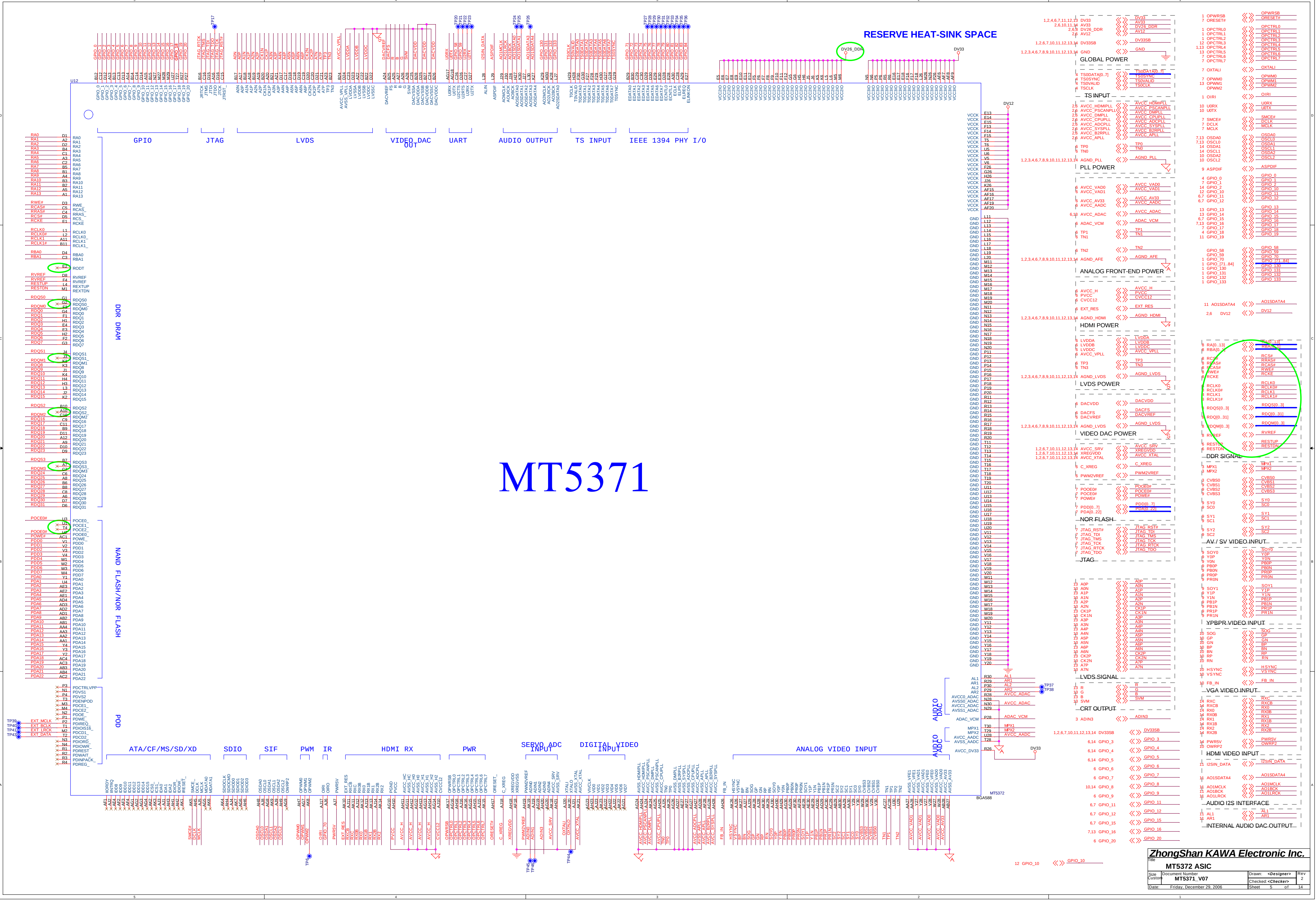
ZhongShan KAWA Electronic Inc.

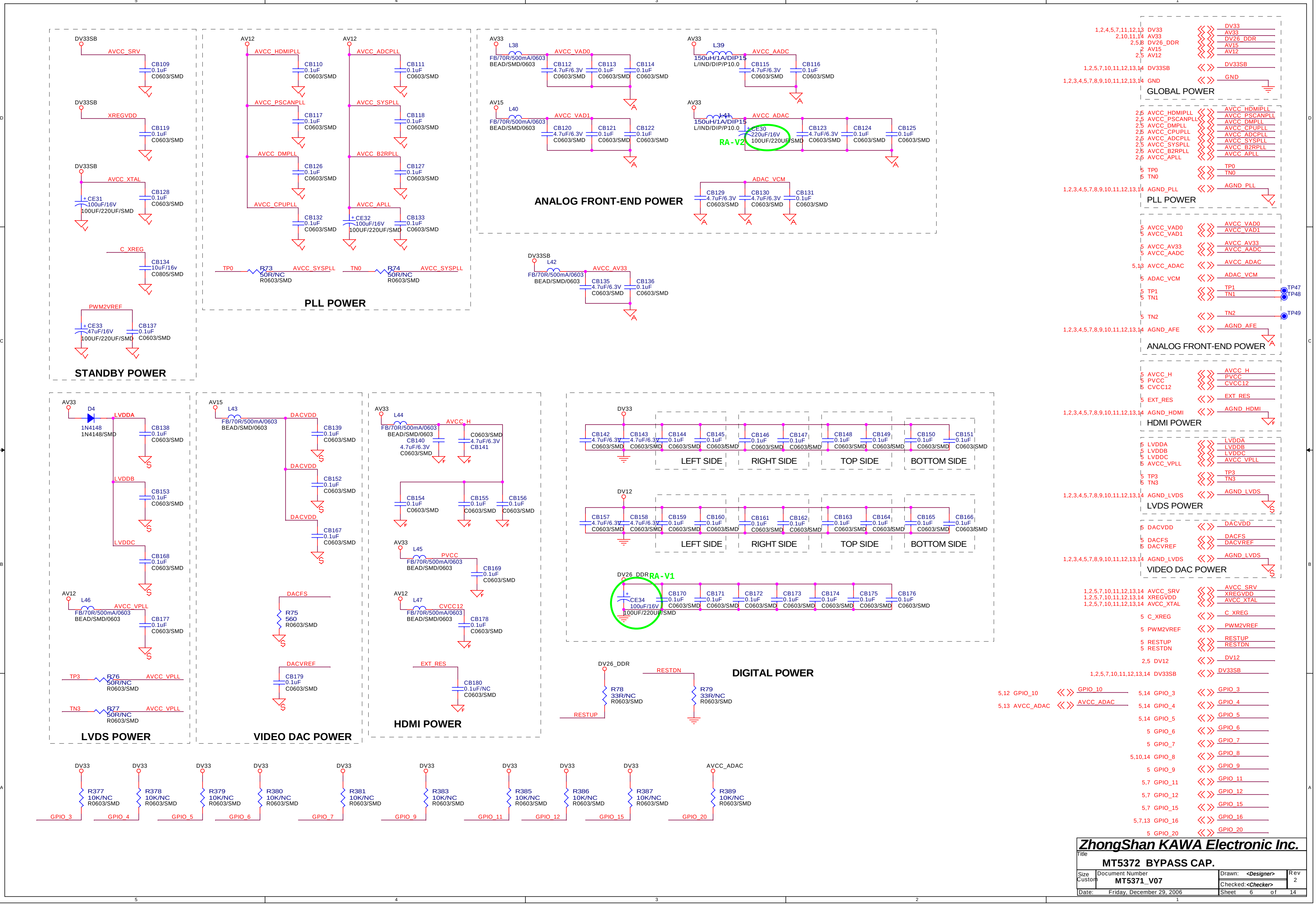
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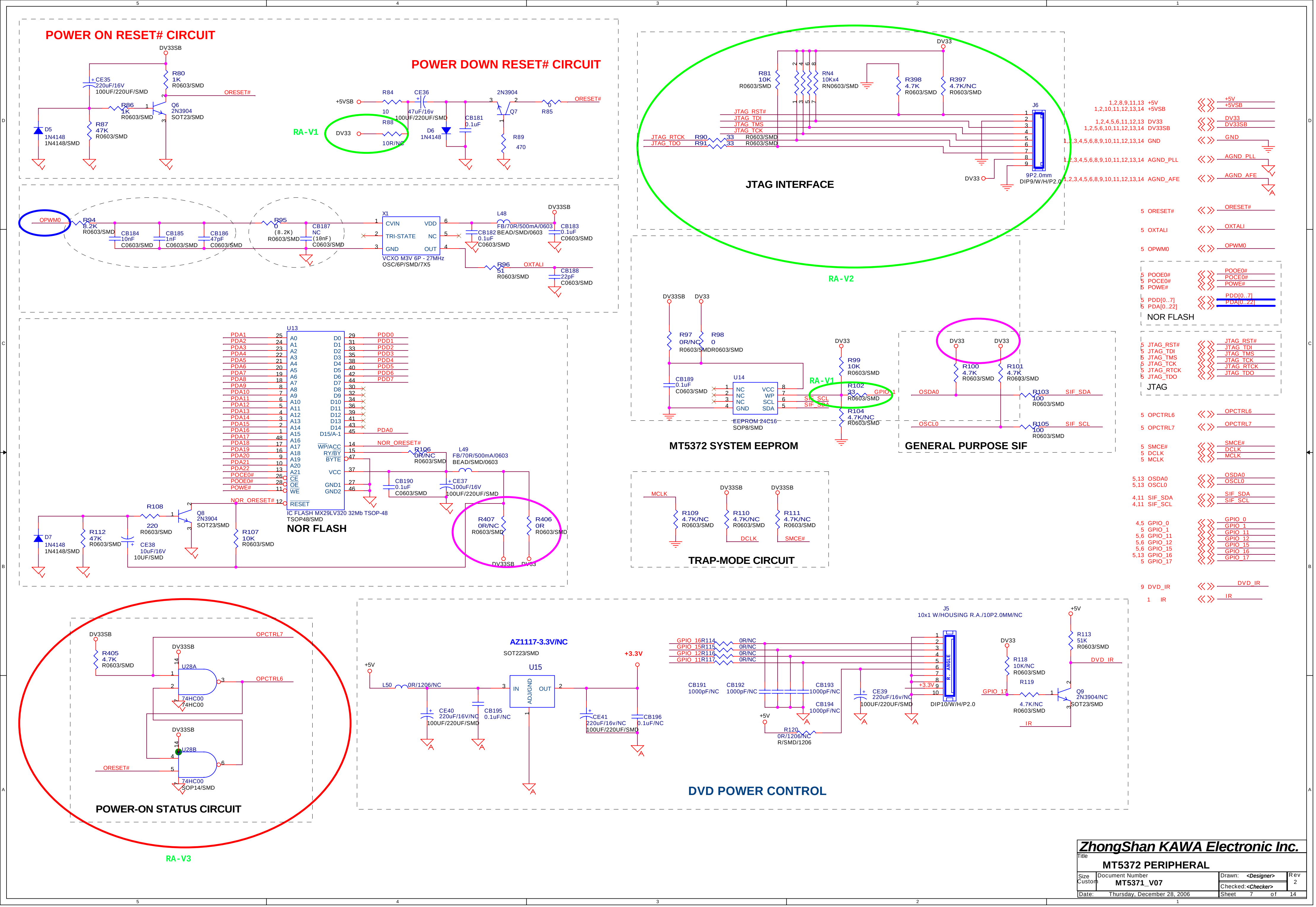

POWER SUPPLY +5V FOR TUNER
U1 L7805 TO220/DIP/SU
POWER SUPPLY +30V FOR SAMSUNG TUNER
Vout = 1.25 x (1 + Rb / Ra)
Regulator AP1522 SOT23-5/SMD
DIODE SMD FHBAS40
RA-V1
1000mA
U2 AP1513/SOP-8
RA-V3
720mA
0.8 x (1+1.2K/2K) = 1.28V
POWER +1V2 FOR MT5372 (DIGITAL)
41mA
POWER +1V2 FOR MT5372 (ANALOG)
U4 AMS1084/ADJ TO-252-3/SMD
28mA
POWER SUPPLY +3V3 (DIGITAL) FOR MT5372
390mA
POWER +3V3 FOR MT5372 (ANALOG)
80mA
POWER SUPPLY +3V3 FOR MT5112
U5 AP1513/SOP-8
900mA
710mA
0.8 x (1+1K/1K) = 1.6V
POWER SUPPLY +1V6 FOR MT5112
U6 AMS1084 TO-252-3/SMD
RA-V2
1.25 x (1+120/110) = 2.6V
POWER +1V8 FOR MT5372 / DDRII
U7 AMS1117-3.3V SOT223/SMD
25mA
1.25 x (1+180/110) = 3.3V
STANDBY POWER +3V3 FOR MT5372
U8 AMS1117/adj SOT223/SMD
88mA
1.25 x (1+22/110) = 1.5V
POWER +1V5 FOR VIDEO FRONT-END1
GLOBAL POWER
ZhongShan KAWA Electronic Inc.
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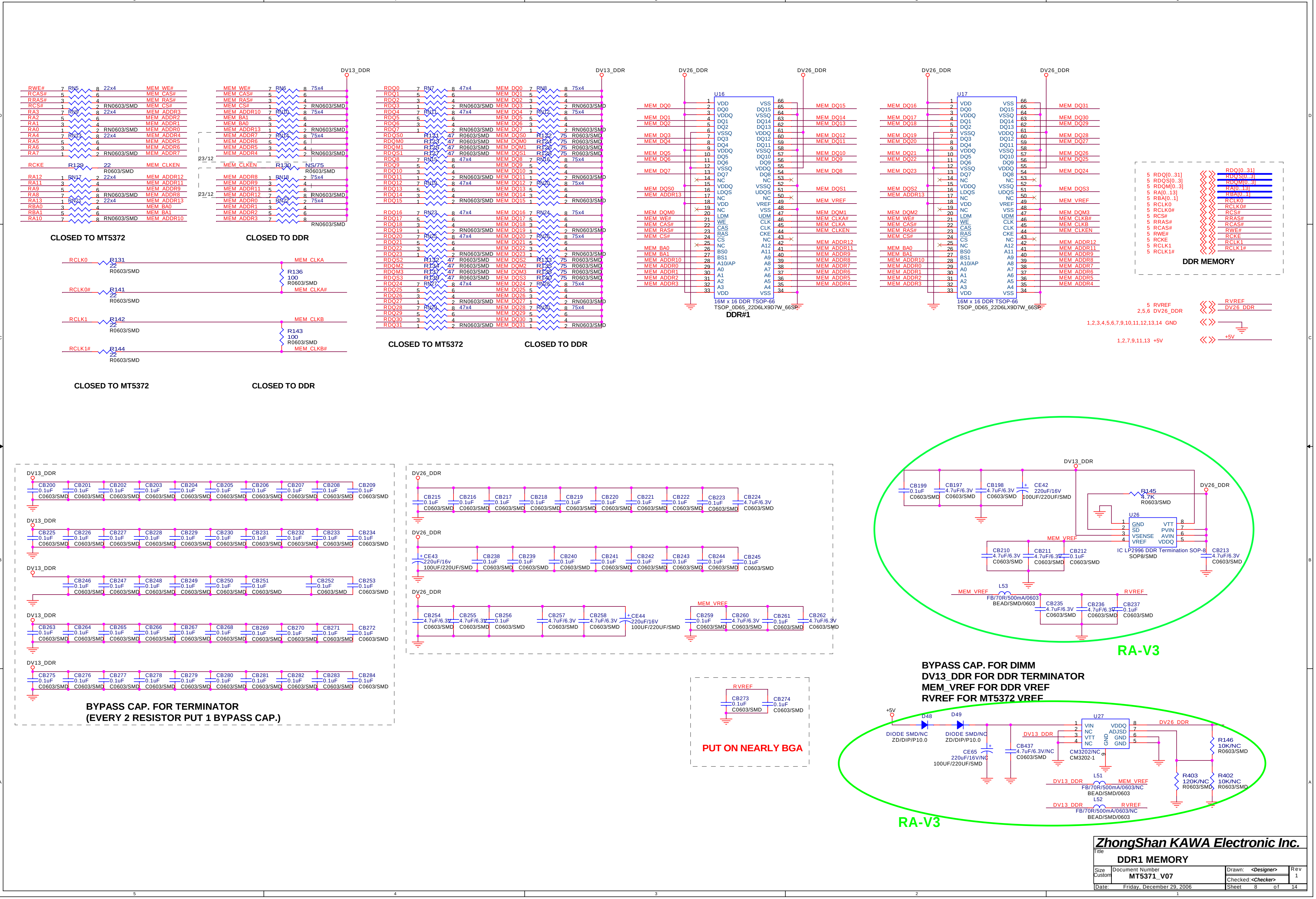

PHILIPS COMBO-TUNER
U9
PORT TUNER FQD1236/F H-5/NC
MK5
RA-V3
R400
0/NC
R0603/SMD
5V_TU
CB49
0.1uF/NC
C0603/SMD
L24
L25
2.2uH/NC
BEAD/SMD/0603
TUNER_SCLO
TUNER_SDAO
IF_AGC
R45
4.7K/NC
R0603/SMD
CB50
10nF/NC
C0603/SMD
R46
R47
NC
R50
4.7K/NC
CB51
0.1uF/NC
R51
0R/NC
FAT_IN+
R52
FAT_IN-
ROUTE SYMMETRICALLY
No Install
TUNER INTERFACE
TUNER - ANALOG OUTPUT
AV / SV VIDEO INPUT
+30V_TUNER
DV33_DM
GND
AGND_AFE
+5V_TUNER
CVBS0
CVBS2
CVBS3
MPX1
MPX2
ADIN3
SY0
SC0
SY1
SC1
SY2
SC2
TUNER_SCL1
TUNER_SDA1
Only for Philips Tuner
SIF LEVEL SHIFTER
R48
10K/NC
R49
10K/NC
QF1
QF2
2N7002/NC
SOT23/SMD
RA-V1
CB52
1000pF
C0603/SMD
MONO
SAMSUNG COMBO-TUNER
U10
PORT TUNER DTVS205CH201A
RA-V2
CB54
100p
CB55
0.1uF
L26
FB/70R/500mA/0603
BEAD/SMD/0603
R55
R57
ROUTE SYMMETRICALLY
CB56
NC
R59
4.7K
CB58
100p
CB59
10nF
Close to Tuner
CB61
CB62
R63
R64
100
CB63
470P
CB64
0.1uF
CE29
470uF/16V
C470UF16V/D8H9G
L27
FB/75R/1A/0805
BEAD/SMD/0805
R404
R399
NEARLY TUNER
NEARLY MT5372
R54
10
R58
100
Q5
2N3904
SOT23/SMD
CE28
47uF/16V
100UF/220UF/SMD
R60
10
R401
0/NC
CB60
47pF
R62
75R/1206
R1206/SMD
R61
100
CB57
47nF
NTSC CVBS
R396
4.7K
CB436
10nF
R67
0
CB65
5.6pF
CB66
15pF
SIF (4.5MHz)
AFT
R53
100K
R56
220K
CB53
0.1uF
R65
4.7K
R66
4.7K
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RESERVE HEAT-SINK SPACE
MT5112AD/BD
TQFP-100
U11
MT5112AD_BD/TQFP100
CLOSE TO MT5112
GLOBAL SIGNAL
TUNER INTERFACE
TS INPUT
RA-V3
MODIFY IN RAV2
TUNER_SDA TUNER_SDA1
TUNER_SCL TUNER_SCL1
Digital 1.8V Bypass Caps
Digital 3.3V Bypass Caps
Analog 3.3V Bypass Caps
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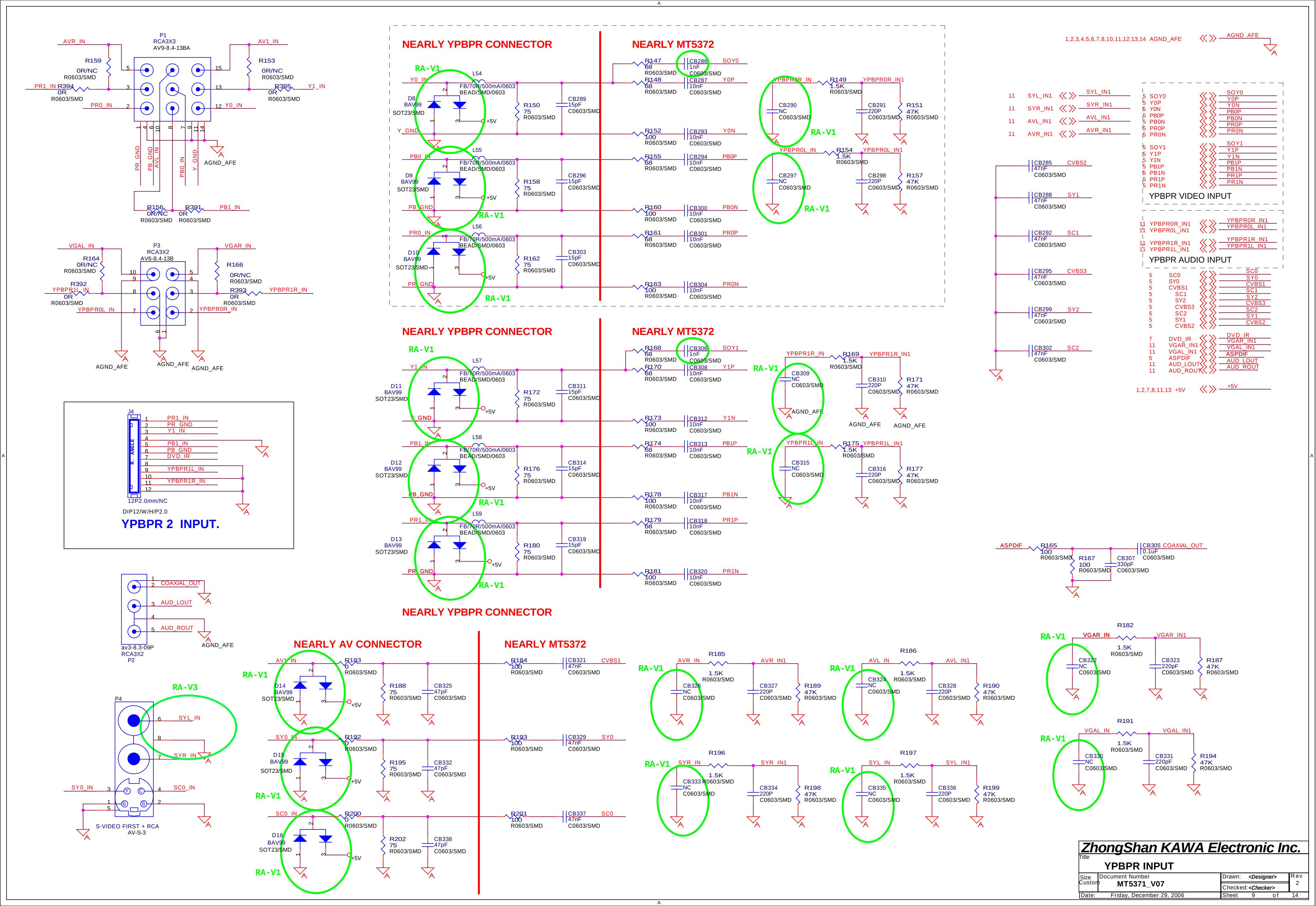

RESERVE HEAT-SINK SPACE
MT5371
U12
GPIO
JTAG
LVDS
VIDEO DAC OUT
UART
AUDIO OUTPUT
TS INPUT
IEEE 1394 PHY I/O
DDR DRAM
NAND FLASH/NOR FLASH
PDD
ATA/CF/MS/SD/XD
SDIO
SIF
PWM
IR
HDMI RX
PWR
SERVO ADC INPUT
DIGITAL VIDEO INPUT
ANALOG VIDEO INPUT
AUDIO DAC
AUDIO ADC
GLOBAL POWER
TS INPUT
PLL POWER
ANALOG FRONT-END POWER
HDMI POWER
LVDS POWER
VIDEO DAC POWER
NOR FLASH
JTAG
LVDS SIGNAL
CRT OUTPUT
DDR SIGNAL
AV / SV VIDEO INPUT
YPBPR VIDEO INPUT
VGA VIDEO INPUT
HDMI VIDEO INPUT
AUDIO I2S INTERFACE
INTERNAL AUDIO DAC OUTPUT
MT5372
BGA588
ZhongShan KAWA Electronic Inc.
Title
MT5372 ASIC
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Date: Friday, December 29, 2006
Sheet 5 of 14

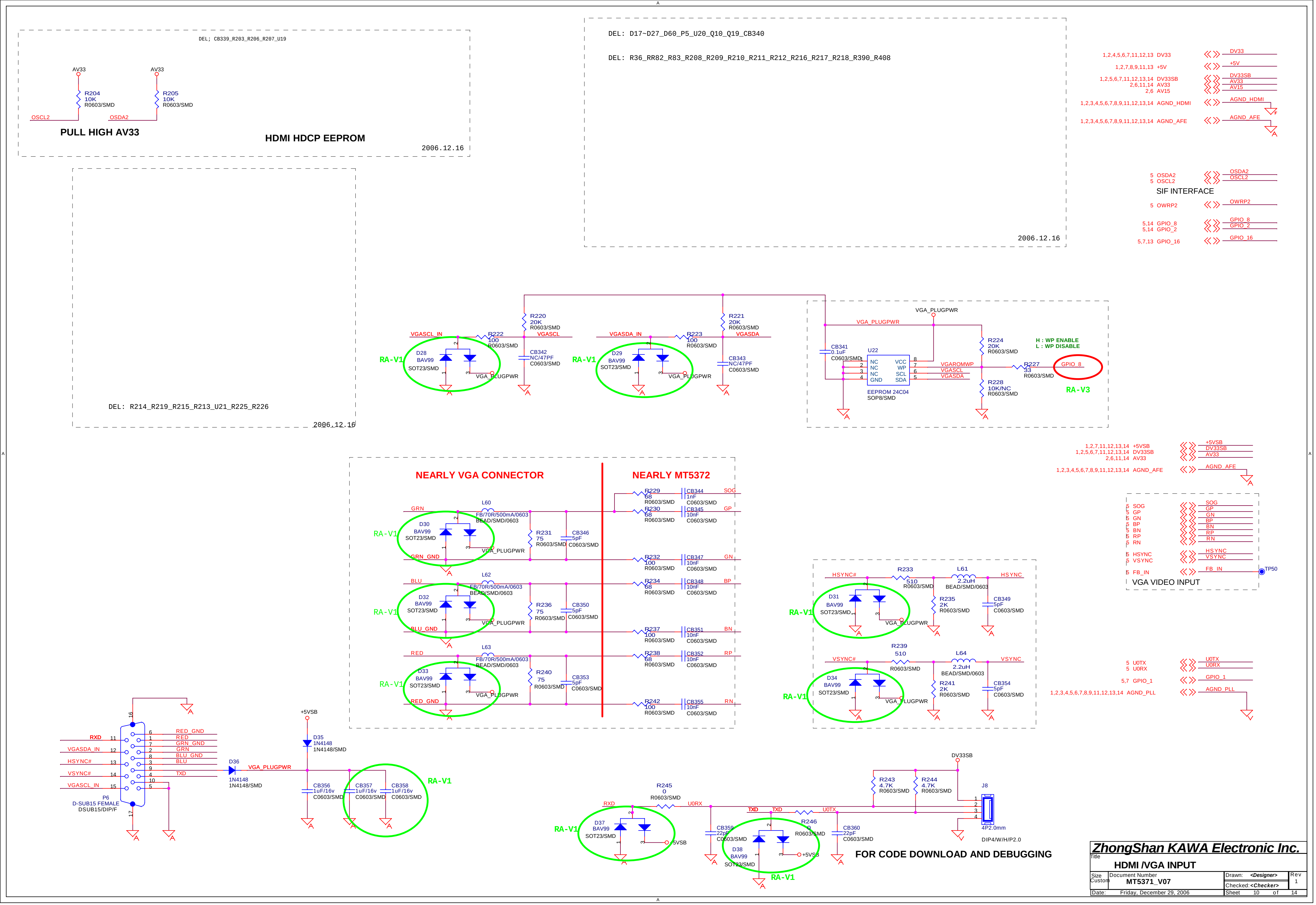

STANDBY POWER
PLL POWER
ANALOG FRONT-END POWER
LVDS POWER
VIDEO DAC POWER
HDMI POWER
DIGITAL POWER
LEFT SIDE
RIGHT SIDE
TOP SIDE
BOTTOM SIDE
GLOBAL POWER
PLL POWER
ANALOG FRONT-END POWER
HDMI POWER
LVDS POWER
VIDEO DAC POWER
RA-V2
RA-V1
ZhongShan KAWA Electronic Inc.
Title
MT5372 BYPASS CAP.
Size Custom
Document Number
MT5371_V07
Drawn: <Designer>
Checked: <Checker>
Rev
2
Date: Friday, December 29, 2006
Sheet 6 of 14

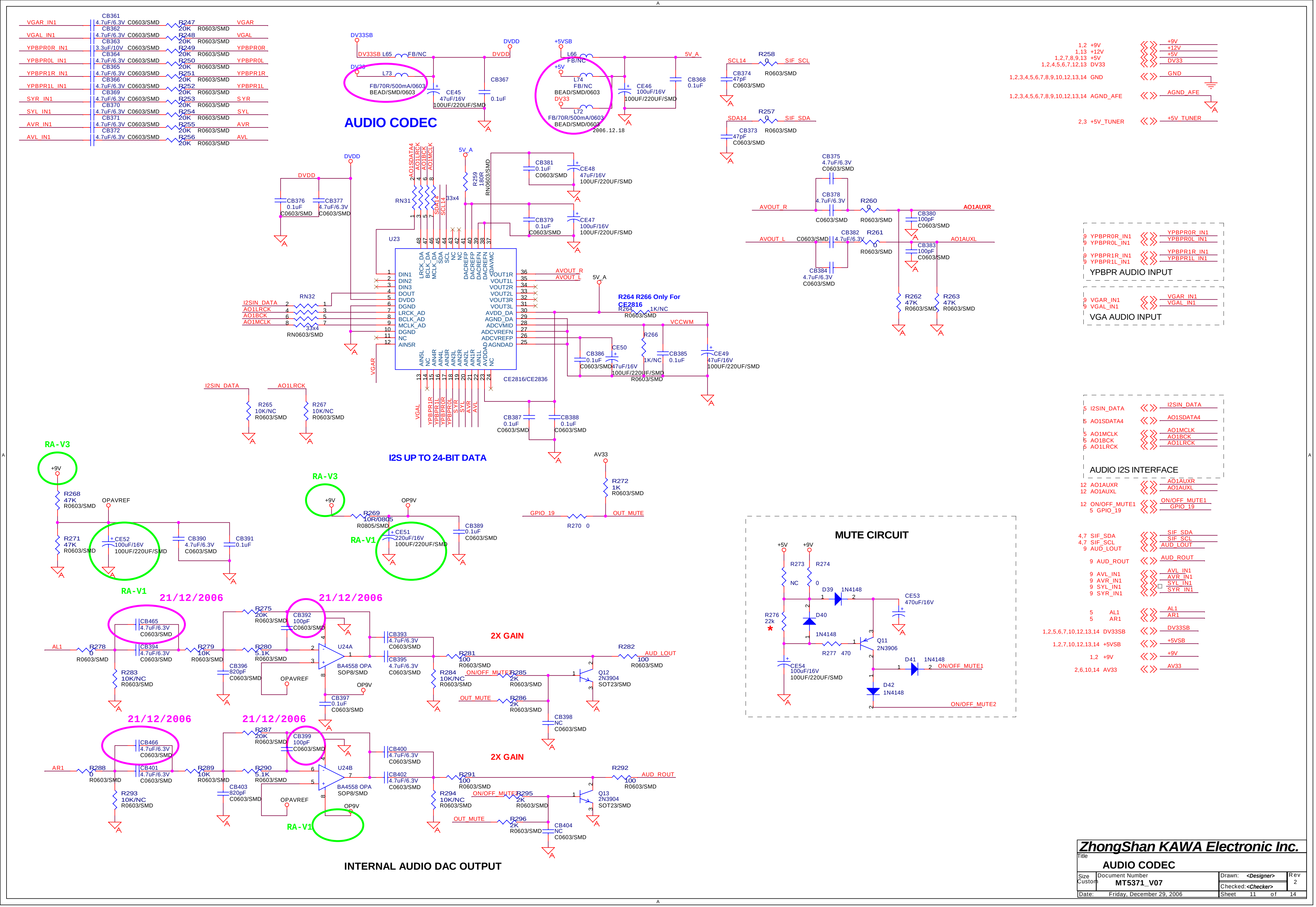

POWER ON RESET# CIRCUIT
POWER DOWN RESET# CIRCUIT
RA-V1
JTAG INTERFACE
RA-V2
NOR FLASH
MT5372 SYSTEM EEPROM
GENERAL PURPOSE SIF
JTAG
TRAP-MODE CIRCUIT
POWER-ON STATUS CIRCUIT
RA-V3
AZ1117-3.3V/NC
DVD POWER CONTROL
ZhongShan KAWA Electronic Inc.
Title
MT5372 PERIPHERAL
Size
Custom
Document Number
MT5371_V07
Drawn:
Checked:
Rev
2
Date:
Thursday, December 28, 2006
Sheet
7
of
14

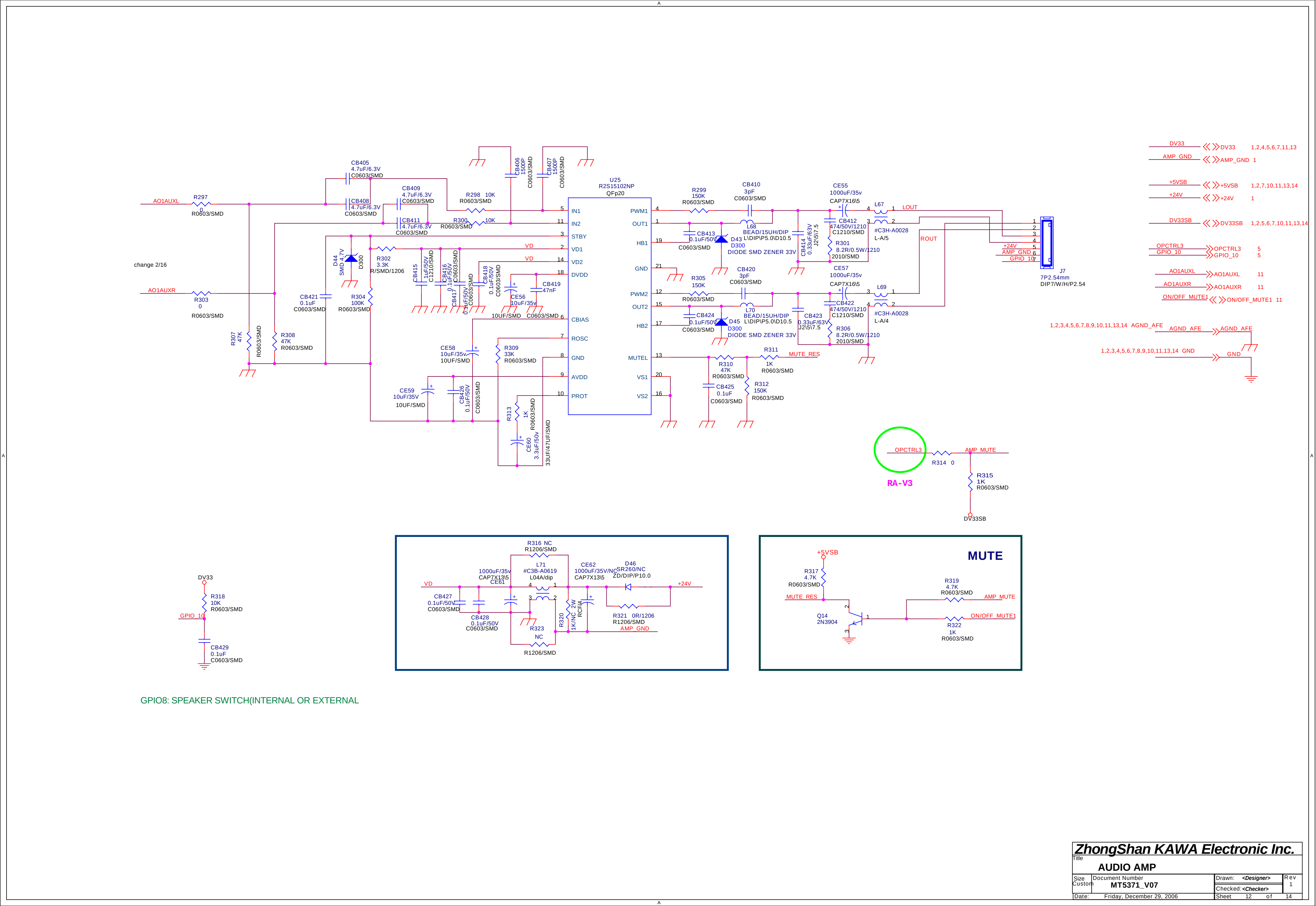


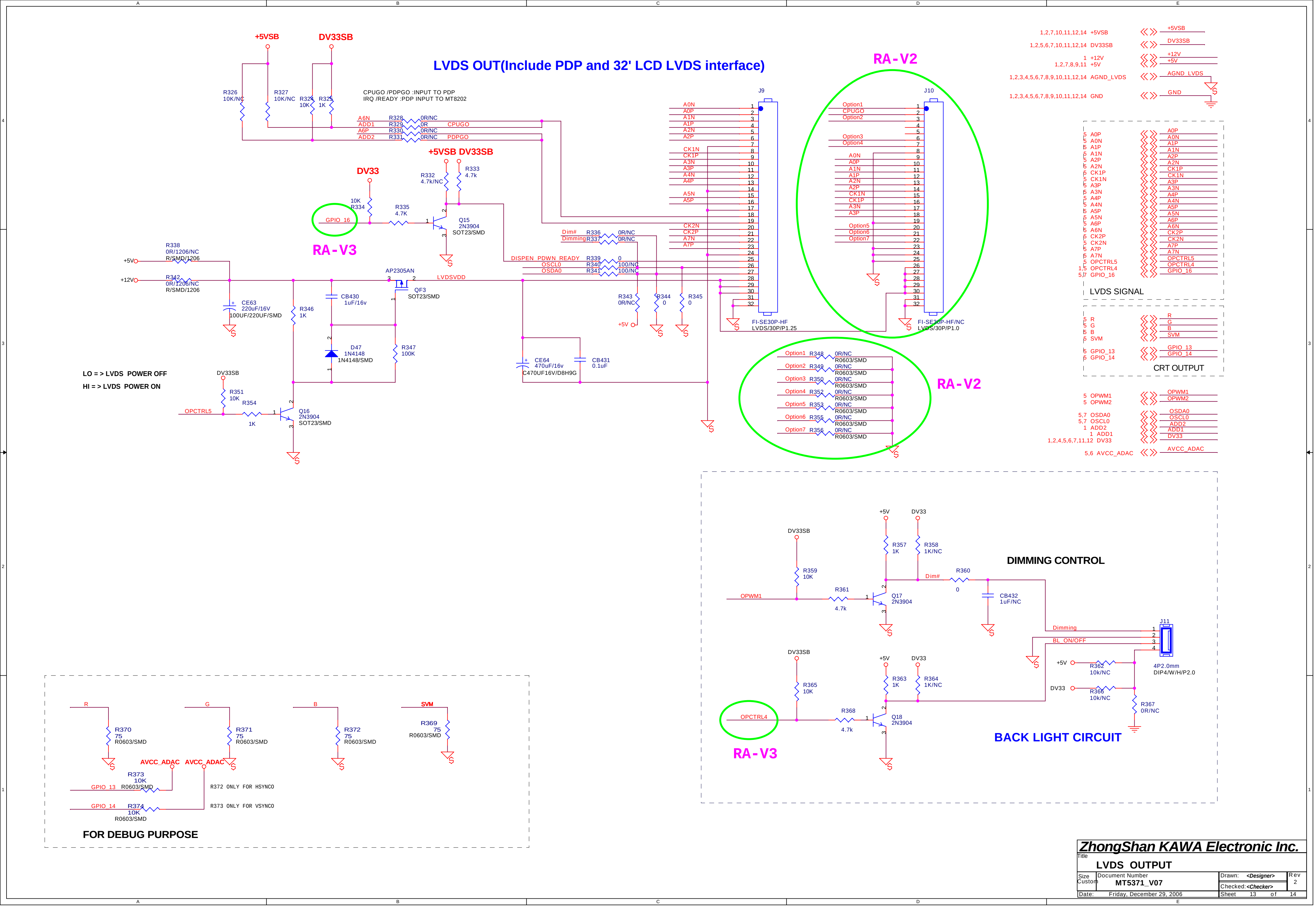
CLOSED TO MT5372
CLOSED TO DDR
CLOSED TO MT5372
CLOSED TO DDR
CLOSED TO MT5372
CLOSED TO DDR
DDR#1
16M x 16 DDR TSOP-66
TSOP_0D65_22D6LX9D7W_66SP
DDR MEMORY
BYPASS CAP. FOR TERMINATOR
(EVERY 2 RESISTOR PUT 1 BYPASS CAP.)
PUT ON NEARLY BGA
BYPASS CAP. FOR DIMM
DV13_DDR FOR DDR TERMINATOR
MEM_VREF FOR DDR VREF
RVREF FOR MT5372 VREF
RA-V3
RA-V3
IC LP2996 DDR Termination SOP-8
ZhongShan KAWA Electronic Inc.
Title
DDR1 MEMORY
Size Custom
Document Number
MT5371_V07
Drawn: <Designer>
Checked: <Checker>
Rev 1
Date: Friday, December 29, 2006
Sheet 8 of 14

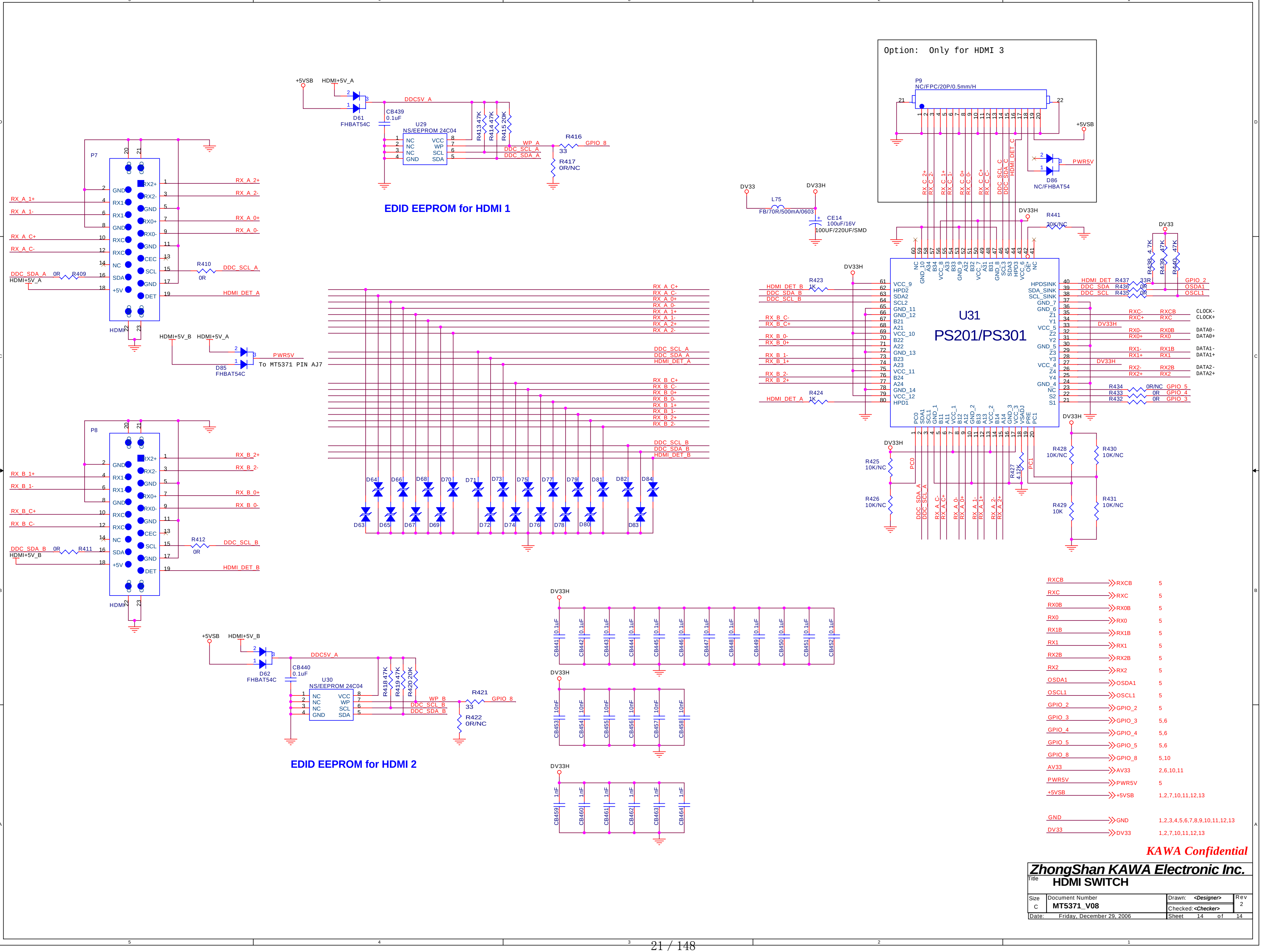

NEARLY YPBPR CONNECTOR
NEARLY MT5372
NEARLY YPBPR CONNECTOR
NEARLY MT5372
NEARLY YPBPR CONNECTOR
NEARLY AV CONNECTOR
NEARLY MT5372
YPBPR VIDEO INPUT
YPBPR AUDIO INPUT
YPBPR 2 INPUT.
S-VIDEO FIRST + RCA
RA-V1
RA-V3
AGND_AFE
ZhongShan KAWA Electronic Inc.
Title
YPBPR INPUT
Size Custom
Document Number
MT5371_V07
Date: Friday, December 29, 2006
Drawn: <Designer>
Checked: <Checker>
Rev 2
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DEL; CB339_R203_R206_R207_U19
PULL HIGH AV33
HDMI HDCP EEPROM
2006.12.16
DEL: D17~D27_D60_P5_U20_Q10_Q19_CB340
DEL: R36_RR82_R83_R208_R209_R210_R211_R212_R216_R217_R218_R390_R408
2006.12.16
DEL: R214_R219_R215_R213_U21_R225_R226
2006.12.16
1,2,4,5,6,7,11,12,13 DV33
1,2,7,8,9,11,13 +5V
1,2,5,6,7,11,12,13,14 DV33SB
2,6,11,14 AV33
2,6 AV15
1,2,3,4,5,6,7,8,9,11,12,13,14 AGND_HDMI
1,2,3,4,5,6,7,8,9,11,12,13,14 AGND_AFE
5 OSDA2
5 OSCL2
SIF INTERFACE
5 OWRP2
5,14 GPIO_8
5,14 GPIO_2
5,7,13 GPIO_16
VGA_PLUGPWR
EEPROM 24C04
SOP8/SMD
H : WP ENABLE
L : WP DISABLE
RA-V1
RA-V3
1,2,7,11,12,13,14 +5VSB
1,2,5,6,7,11,12,13,14 DV33SB
2,6,11,14 AV33
1,2,3,4,5,6,7,8,9,11,12,13,14 AGND_AFE
NEARLY VGA CONNECTOR
NEARLY MT5372
5 SOG
5 GP
5 GN
5 BP
5 BN
5 RP
5 RN
5 HSYNC
5 VSYNC
5 FB_IN
VGA VIDEO INPUT
5 U0TX
5 U0RX
5,7 GPIO_1
1,2,3,4,5,6,7,8,9,11,12,13,14 AGND_PLL
P6
D-SUB15 FEMALE
DSUB15/DIP/F
J8
4P2.0mm
DIP4/W/H/P2.0
FOR CODE DOWNLOAD AND DEBUGGING
ZhongShan KAWA Electronic Inc.
Title
HDMI /VGA INPUT
Size Custom
Document Number
MT5371_V07
Drawn: <Designer>
Checked: <Checker>
Rev 1
Date: Friday, December 29, 2006
Sheet 10 of 14

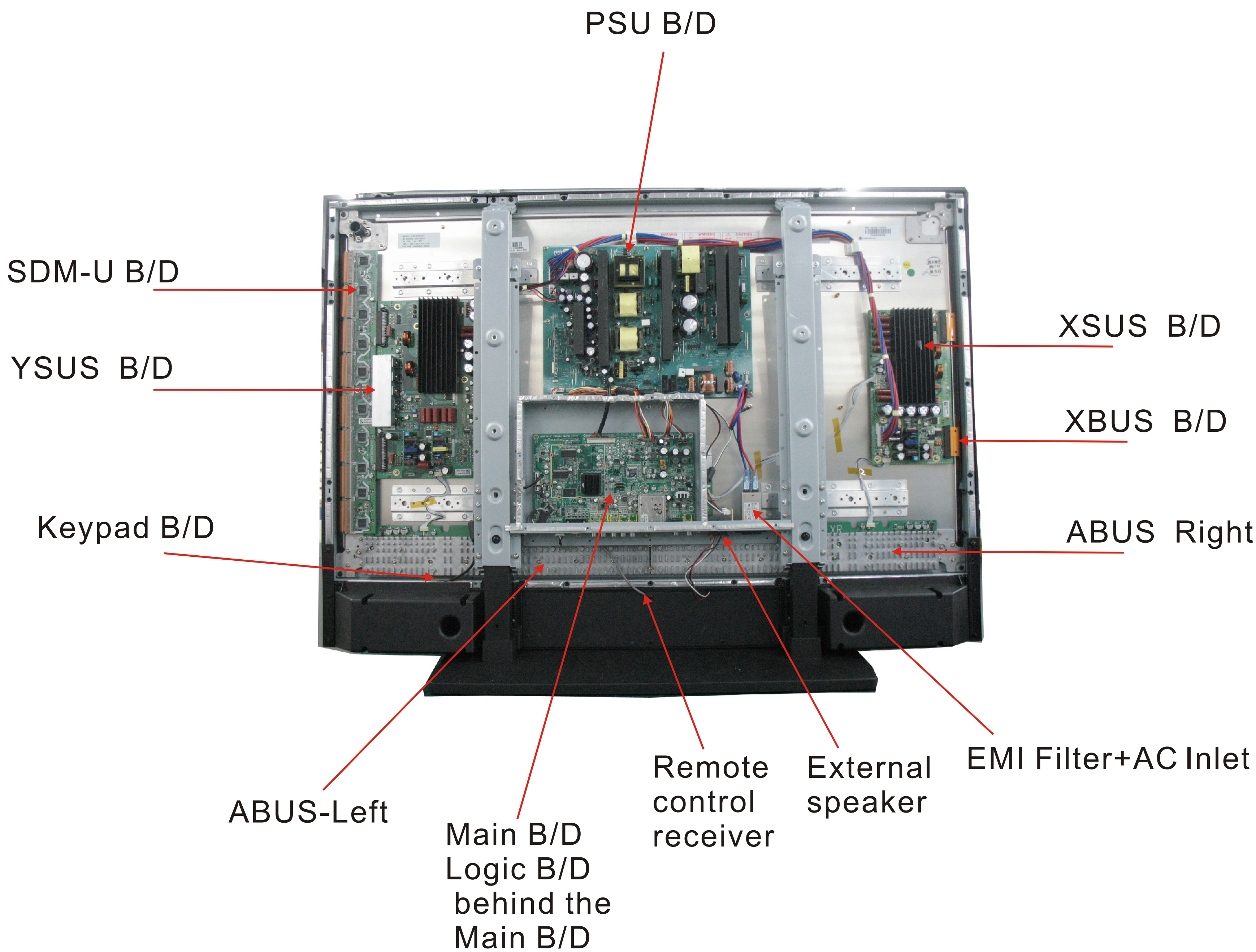

AUDIO CODEC
I2S UP TO 24-BIT DATA
INTERNAL AUDIO DAC OUTPUT
2X GAIN
2X GAIN
MUTE CIRCUIT
YPBPR AUDIO INPUT
VGA AUDIO INPUT
AUDIO I2S INTERFACE
R264 R266 Only For CE2816
CE2816/CE2836
RA-V3
RA-V1
21/12/2006
2006.12.18
ZhongShan KAWA Electronic Inc.
Title
AUDIO CODEC
Size Custom
Document Number
MT5371_V07
Rev 2
Drawn: <Designer>
Checked: <Checker>
Date: Friday, December 29, 2006
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U25
R2S15102NP
QFp20
IN1
IN2
STBY
VD1
VD2
DVDD
CBIAS
ROSC
GND
AVDD
PROT
PWM1
OUT1
HB1
GND
PWM2
OUT2
HB2
MUTEL
VS1
VS2
AO1AUXL
AO1AUXR
R297
R0603/SMD
R303
0
R0603/SMD
change 2/16
CB405
4.7uF/6.3V
C0603/SMD
CB408
4.7uF/6.3V
C0603/SMD
CB409
4.7uF/6.3V
C0603/SMD
CB411
4.7uF/6.3V
C0603/SMD
R298 10K
R0603/SMD
R300 10K
R0603/SMD
CB406
1500P
C0603/SMD
CB407
1500P
C0603/SMD
D44
SMD 4.7V
D300
R302
3.3K
R/SMD/1206
VD
CB415
1uF/50V
C1210/SMD
CB416
0.1uF/50V
C0603/SMD
CB417
0.1uF/50V
C0603/SMD
CB418
0.1uF/50V
C0603/SMD
CE56
10uF/35v
10UF/SMD
CB419
47nF
C0603/SMD
CB421
0.1uF
C0603/SMD
R304
100K
R0603/SMD
R307
47K
R0603/SMD
R308
47K
R0603/SMD
CE58
10uF/35v
10UF/SMD
R309
33K
R0603/SMD
CE59
10uF/35V
10UF/SMD
CB426
0.1uF/50V
C0603/SMD
R313
1K
R0603/SMD
CE60
3.3uF/50v
33UF/47UF/SMD
R299
150K
R0603/SMD
CB410
3pF
C0603/SMD
CB413
0.1uF/50V
C0603/SMD
D43
D300
DIODE SMD ZENER 33V
L68
BEAD/15UH/DIP
L\DIP\P5.0\D10.5
CB414
0.33uF/63V
J2\5\7.5
CE55
1000uF/35v
CAP7X16\5
CB412
474/50V/1210
C1210/SMD
R301
8.2R/0.5W/1210
2010/SMD
L67
#C3H-A0028
L-A/5
LOUT
ROUT
R305
150K
R0603/SMD
CB420
3pF
C0603/SMD
CB424
0.1uF/50V
C0603/SMD
D45
D300
DIODE SMD ZENER 33V
L70
BEAD/15UH/DIP
L\DIP\P5.0\D10.5
CB423
0.33uF/63V
J2\5\7.5
CE57
1000uF/35v
CAP7X16\5
CB422
474/50V/1210
C1210/SMD
R306
8.2R/0.5W/1210
2010/SMD
L69
#C3H-A0028
L-A/4
R310
47K
R0603/SMD
R311
1K
R0603/SMD
MUTE_RES
CB425
0.1uF
C0603/SMD
R312
150K
R0603/SMD
+24V
AMP_GND
GPIO_10
J7
7P2.54mm
DIP7/W/H/P2.54
DV33
AMP_GND
+5VSB
+24V
DV33SB
OPCTRL3
GPIO_10
AO1AUXL
AO1AUXR
ON/OFF_MUTE1
DV33 1,2,4,5,6,7,11,13
AMP_GND 1
+5VSB 1,2,7,10,11,13,14
+24V 1
DV33SB 1,2,5,6,7,10,11,13,14
OPCTRL3 5
GPIO_10 5
AO1AUXL 11
AO1AUXR 11
ON/OFF_MUTE1 11
1,2,3,4,5,6,7,8,9,10,11,13,14 AGND_AFE
AGND_AFE
AGND_AFE
1,2,3,4,5,6,7,8,9,10,11,13,14 GND
GND
OPCTRL3
R314 0
AMP_MUTE
R315
1K
R0603/SMD
DV33SB
RA-V3
R316 NC
R1206/SMD
L71
#C3B-A0619
L04A/dip
1000uF/35v
CAP7X13\5
CE61
CE62
1000uF/35V/NC
CAP7X13\5
D46
SR260/NC
ZD/DIP/P10.0
VD
+24V
CB427
0.1uF/50V
C0603/SMD
CB428
0.1uF/50V
C0603/SMD
R323
NC
R1206/SMD
R320
1K/NC 2W
RCF/4
R321 0R/1206
R1206/SMD
AMP_GND
+5VSB
MUTE
R317
4.7K
R0603/SMD
MUTE_RES
Q14
2N3904
R319
4.7K
R0603/SMD
AMP_MUTE
ON/OFF_MUTE1
R322
1K
R0603/SMD
DV33
R318
10K
R0603/SMD
GPIO_10
CB429
0.1uF
C0603/SMD
GPIO8: SPEAKER SWITCH(INTERNAL OR EXTERNAL
ZhongShan KAWA Electronic Inc.
Title
AUDIO AMP
Size Custom
Document Number
MT5371_V07
Drawn: <Designer>
Checked: <Checker>
Rev 1
Date: Friday, December 29, 2006
Sheet 12 of 14


LVDS OUT(Include PDP and 32' LCD LVDS interface)
+5VSB
DV33SB
RA-V2
RA-V3
CPUGO /PDPGO :INPUT TO PDP
IRQ /READY :PDP INPUT TO MT8202
R326 10K/NC
R327 10K/NC
R324 10K
R325 1K
A6N R328 0R/NC
ADD1 R329 0R CPUGO
A6P R330 0R/NC
ADD2 R331 0R/NC PDPGO
+5VSB DV33SB
DV33
R332 4.7k/NC
R333 4.7k
10K R334
R335 4.7K
GPIO_16
Q15 2N3904 SOT23/SMD
R338 0R/1206/NC R/SMD/1206
R342 0R/1206/NC R/SMD/1206
+5V
+12V
CE63 220uF/16V 100UF/220UF/SMD
R346 1K
AP2305AN
QF3 SOT23/SMD
LVDSVDD
CB430 1uF/16v
D47 1N4148 1N4148/SMD
R347 100K
Dim# R336 0R/NC
Dimming R337 0R/NC
DISPEN_PDWN_READY R339 0
OSCL0 R340 100/NC
OSDA0 R341 100/NC
R343 0R/NC
R344 0
R345 0
CE64 470uF/16v C470UF16V/D8H9G
CB431 0.1uF
LO = > LVDS POWER OFF
HI = > LVDS POWER ON
DV33SB
R351 10K
R354 1K
OPCTRL5
Q16 2N3904 SOT23/SMD
J9
FI-SE30P-HF LVDS/30P/P1.25
J10
FI-SE30P-HF/NC LVDS/30P/P1.0
Option1 CPUGO Option2 Option3 Option4 Option5 Option6 Option7
Option1 R348 0R/NC R0603/SMD
Option2 R349 0R/NC R0603/SMD
Option3 R350 0R/NC R0603/SMD
Option4 R352 0R/NC R0603/SMD
Option5 R353 0R/NC R0603/SMD
Option6 R355 0R/NC R0603/SMD
Option7 R356 0R/NC R0603/SMD
1,2,7,10,11,12,14 +5VSB
1,2,5,6,7,10,11,12,14 DV33SB
1 +12V
1,2,7,8,9,11 +5V
1,2,3,4,5,6,7,8,9,10,11,12,14 AGND_LVDS
1,2,3,4,5,6,7,8,9,10,11,12,14 GND
LVDS SIGNAL
CRT OUTPUT
5 OPWM1
5 OPWM2
5,7 OSDA0
5,7 OSCL0
1 ADD2
1 ADD1
1,2,4,5,6,7,11,12 DV33
5,6 AVCC_ADAC
DIMMING CONTROL
R357 1K
R358 1K/NC
R359 10K
R360 0
R361 4.7k
OPWM1
Q17 2N3904
CB432 1uF/NC
Dimming
BL_ON/OFF
J11 4P2.0mm DIP4/W/H/P2.0
R362 10k/NC
R366 10k/NC
R367 0R/NC
R363 1K
R364 1K/NC
R365 10K
R368 4.7k
OPCTRL4
Q18 2N3904
BACK LIGHT CIRCUIT
R370 75 R0603/SMD
R371 75 R0603/SMD
R372 75 R0603/SMD
R369 75 R0603/SMD
SVM
AVCC_ADAC
R373 10K R0603/SMD
GPIO_13
GPIO_14
R374 10K R0603/SMD
R372 ONLY FOR HSYNCO
R373 ONLY FOR VSYNCO
FOR DEBUG PURPOSE
ZhongShan KAWA Electronic Inc.
Title LVDS OUTPUT
Size Custom
Document Number MT5371_V07
Rev 2
Drawn: <Designer>
Checked: <Checker>
Date: Friday, December 29, 2006
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Option: Only for HDMI 3
P9
NC/FPC/20P/0.5mm/H
EDID EEPROM for HDMI 1
EDID EEPROM for HDMI 2
U29
NS/EEPROM 24C04
U30
NS/EEPROM 24C04
D61
FHBAT54C
D62
FHBAT54C
D85
FHBAT54C
D86
NC/FHBAT54
To MT5371 PIN AJ7
P7
P8
HDMI
U31
PS201/PS301
L75
FB/70R/500mA/0603
CE14
100uF/16V
100UF/220UF/SMD
CLOCK-
CLOCK+
DATA0-
DATA0+
DATA1-
DATA1+
DATA2-
DATA2+
RXCB 5
RXC 5
RX0B 5
RX0 5
RX1B 5
RX1 5
RX2B 5
RX2 5
OSDA1 5
OSCL1 5
GPIO_2 5
GPIO_3 5,6
GPIO_4 5,6
GPIO_5 5,6
GPIO_8 5,10
AV33 2,6,10,11
PWR5V 5
+5VSB 1,2,7,10,11,12,13
GND 1,2,3,4,5,6,7,8,9,10,11,12,13
DV33 1,2,7,10,11,12,13
KAWA Confidential
ZhongShan KAWA Electronic Inc.
Title
HDMI SWITCH
Size C
Document Number
MT5371_V08
Drawn: <Designer>
Checked: <Checker>
Rev 2
Date: Friday, December 29, 2006
Sheet 14 of 14

Parts position



Basic Operations & Circuit Description

MODULE

There are 1 pcs panel and 9 pcs PCB including 2 pcs X/Y Sustainer board, 1 pcs XBUS board, 1 pcs SDM-U board, 1 pcs SDM-D board, 2 pcs ABUS (L and R) board, 1 pcs Logic (Signal Input) board, and 1 pcs PSU board in the Module.

SET

There are 5 pcs PCBs including 1 pcs Main board, 1 pcs Keypad board, 1 pcs Remote Control Receiver board, 1 pcs L/R Speakers and 1 pcs Sub PSU board in the SET.

Basic operation of Plasma Display

1. After turning on power switch, PSU board sends 5Vst-by Volt to Main IC MT5371 waiting for ON signals from Key Switch or Remote Receiver.

2. When the ON signal from Key Switch or Remote Receiver is detected, MT5371 will send ON Control signals to Power. Then Sub PSU sends 5Vsc, 9Vsc, 24V to PCBs working. This time Logic Board will send signals to Panel by X/Y SUS Board, OSD on the panel and display available signal. If the audio signals input, them will be amplified by Audio AMP and transmitted to Speakers.

3. If some abnormal signals are detected (for example: over volts, over current, over temperature and under volts), the system will be shut down by Power off.

PCB function

1. **PSU and Sub PSU:**
   (1). Input voltage: AC 120V, 60Hz.
   (2). To provide power for PCBs.
2. **Main board: To converter S signals, AV signals, Y Pb/Cb Pr/Cr signals, HDMI signals and D-SUB signals to digital ones and to transmit to Control board.**
3. **Logic board: Dealing with the digital signal for output to panel.**
4. **Y-Sustainer / X-Sustainer board:**
   (1). Receiving the signals from Logic and high voltage supply.
   (2). Output scanning waveform for Module.
5. **SDM-U and SDM-D board: Receive signal from Y sustainer, output horizontal scanning waveform to the panel.**
6. **ABUS (L and R) extension board: Output addressing signals.**

PCB failure analysis

1. LOGIC: a. Abnormal noise on screen. b. No picture.
2. MAIN : a. Lacking color, Bad color scale.
   b. No voice.
   c. No picture but with signals output and OSD.
   d. Abnormal noise on screen.
3. PSU and Sub PSU: No picture, no power output.
4. X - Sustainer: a. No picture.
   b. Color not enough.
   c. Flash on screen.
5. Y - Sustainer: Darker picture with signals.
6. X/Y - Sustainer: The component working temperature is about 55°C.
   If the temperature rises abnormal, this may be a error point.

Main IC Specifications

- MT537x Application Note

- MT5112BD

- CE2836
  24-bit, 192KHz. CODEC: 6 ch DAC, 5 Input Mux Stereo ADC

- R2S15102NP
  Digital Power Amplifier R2S15102NP

MT537x Application Note

Specifications are subject to change without notice

MT537x Application Note

V 0.5

Specifications are subject to change without notice

1. Revision History

Date	Description	Version
2006/05/18	Initial Version (Draft)	V.0.3
2006/05/27	Updated Power Load Power On/Off Timing	V0.4
2006/06/06	Update On/Off Timing	V0.5

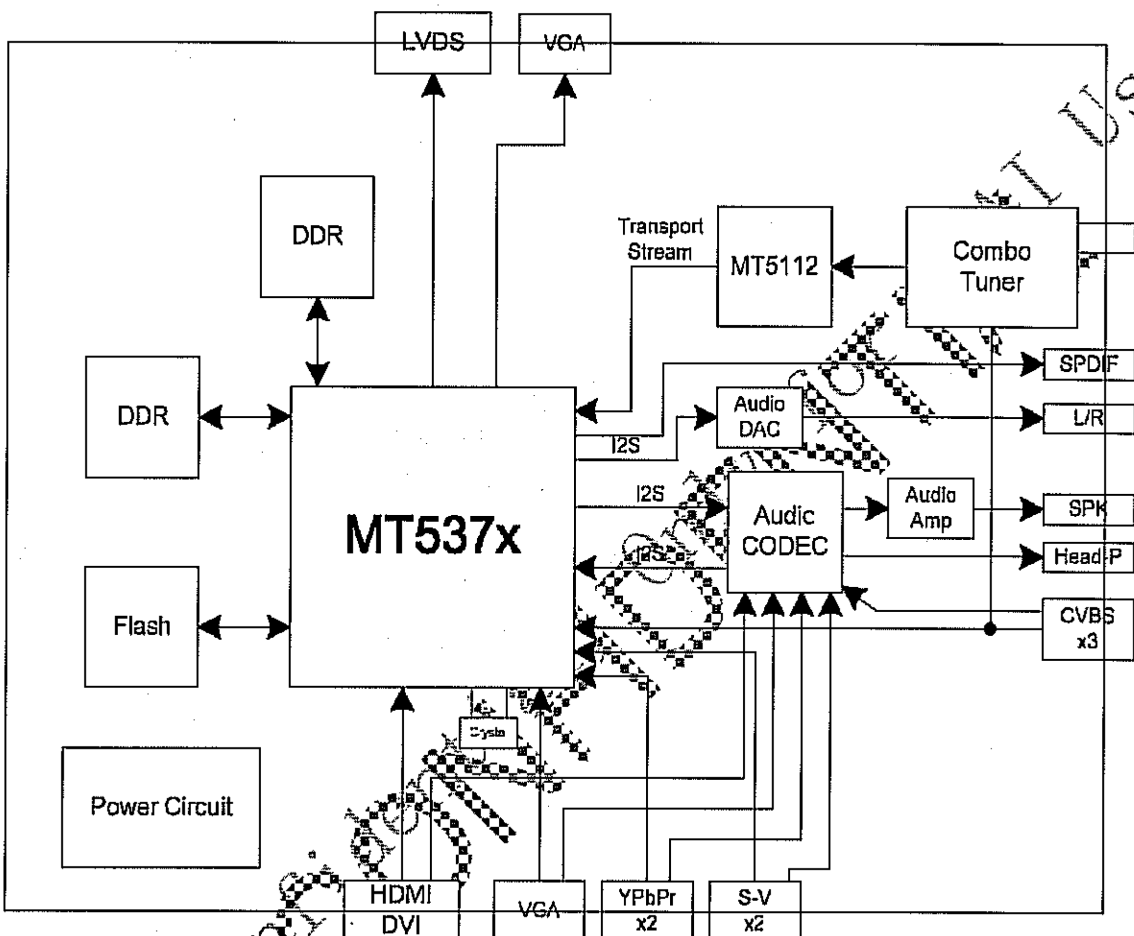
Specifications are subject to change without notice

2. MT537x Feature

MediaTek MT537x is a highly integrated SOC which include DTV backend decoder and TV controller. MT537x support transport de-multiplexer, MPEG-2 video decoder, AC3 audio decoder, LVDS transmitter, TV decoder. The MT537x enables consumer electronics manufactures to build high quality, feature-rich DTV.
World-Leading Video Technology: MT537x embedded the MDDi deinterlacer to generate very smooth picture quality for motion. 3D comb filter also recovery high detail for still picture. The special color processing technology provided favorite and natural color for TV.
Rich Features for High Value Product: To enrich the features of DTV, MT537x support HDMI receiver, PIP/POP, memory card and DV decoding.
Credible Analog Technology: The MT537x integrated with high speed VGA ADC, high resolution Video/Audio ADC, 90db Audio DAC and 12-bit Video DAC. It will provide very fine quality for TV.

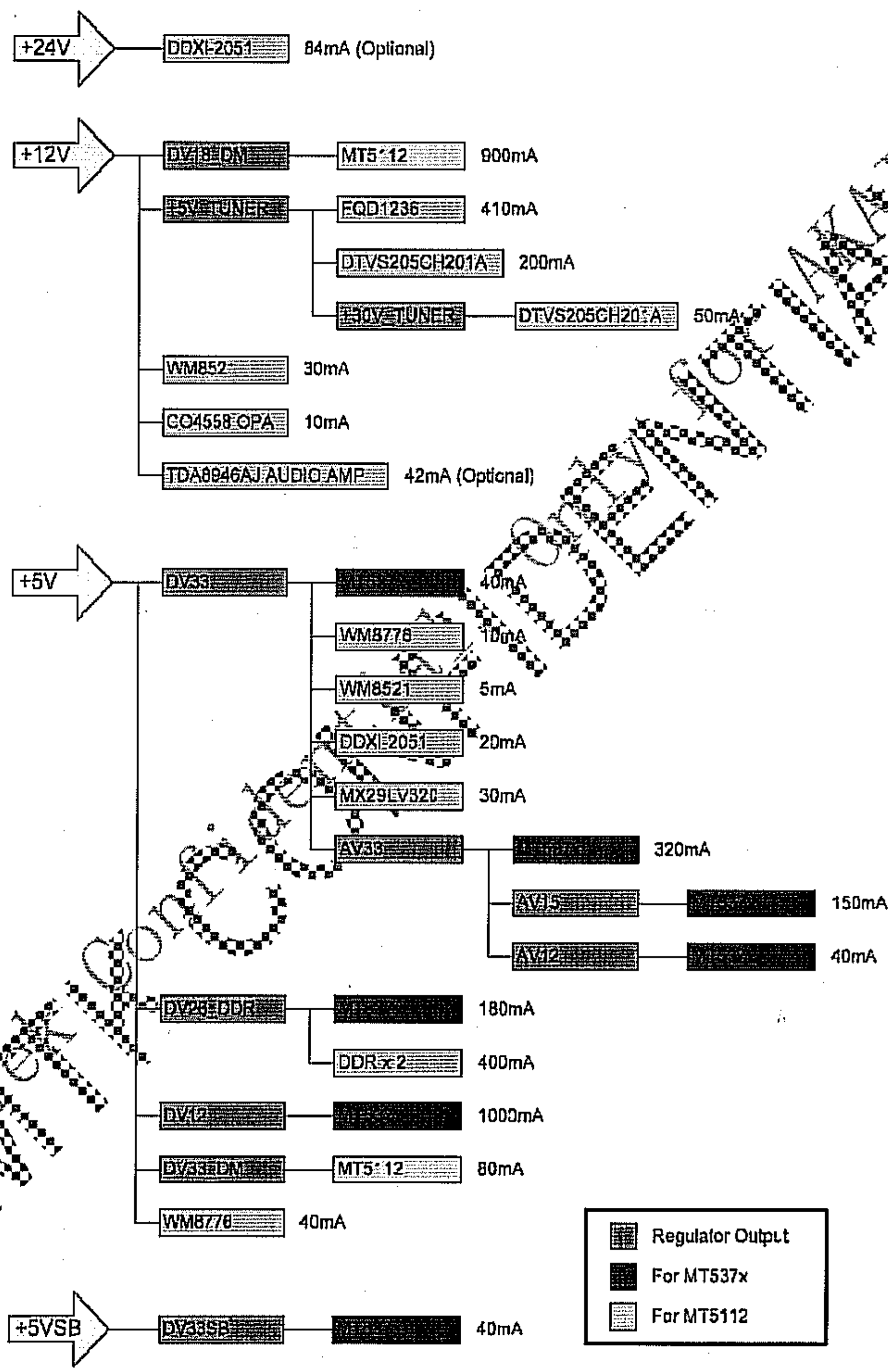
3. DTV System Block (Reference Design)

Specifications are subject to change without notice



4. DTV System Power Load (Based on Reference Design)

Specifications are subject to change without notice



Specifications are subject to change without notice

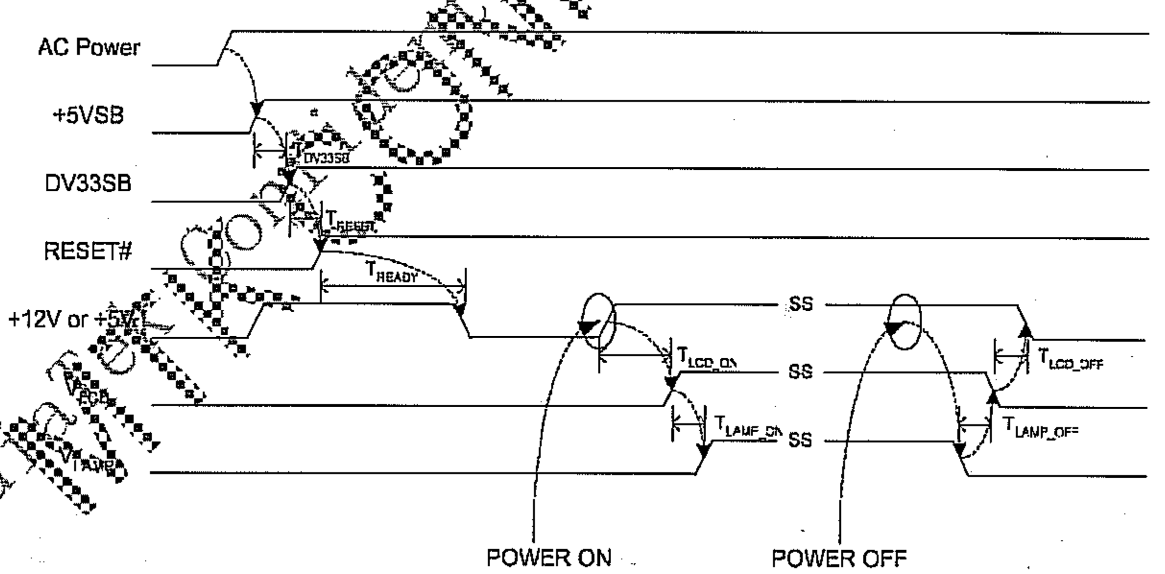
5. MT537x Power Consumption

Under Measurement

Power	Current (mA)	Power Consumption (mW)	PS
DV33	40	132	
AV33	320	1056	
DV26	180	468	
AV15	150	225	
DV12	1000	1200	
AV12	40	48	
DV33SB	40	132	

Note :
Due to We are Under Integration, the Power Consumption Just for Reference. The Power may Increase after Full Function Play.

6. MT537x Power On / Off Timing



Description	Symbol	Min	TPY	Max	Units	PS
DV33SB Power Ready	T_{DV33SB}	0			ms	

Specifications are subject to change without notice

Power-on Reset Period	T_{RESET}	10			ms	
MT537x Boot Ready	T_{READY}		20		ms	
LCD Power On	$T_{LCD\ ON}$				ms	Depend-on Panel
LCD Lamp On	$T_{LAMP\ ON}$				ms	Depend-on Panel
LCD Lamp Off	$T_{LAMP\ OFF}$				ms	Depend-on Panel
LCD Power Off	T_{LCD_OFF}				ms	Depend-on Panel

7. MT537x Diagnostic Program CLI Commands

Under Development

- cd – change current directory
  ex. cd.av – change the directory to AV directory
- do – repeat command
  do "number of times"
  ex. do
- read (r) – memory read
  r "address" "number of bytes"
  ex. r 0x2000d068 8 ← read 8 bytes data from 0x2000d068 address
- write (w) – memory write
  w "address" "data"
  ex. w 0x2000d068 0x12345678 ← write 0x12345678 data to 0x2000d068 address
- basic (b) – basic command
  - stop - stop RS232 transparent mode (set to normal mode)
    ex. b.stop ← set RS232 to normal mode
  - sv – system mode detection
    ex. b.sv ← to detect the system mode
  - reboot – system reboot / restart
    ex. b.reboot ← reboot the system

8. MT537x Debug Flow

Under Development

9. MT537x NOR Flash Supported

Specifications are subject to change without notice

Brand	IC Order Number	Size	Description
MXIC	MX29LV320ABTC-70	32MBits	Under Testing
MXIC	MX29LV320ABTC-90	32MBits	Under Testing
MXIC	MX29LV320ATTC-70	32MBits	Under Testing
MXIC	MX29LV320ATTC-90	32MBits	Under Testing
MXIC	MX29LV320BBTC-70	32MBits	Under Testing
MXIC	MX29LV320BBTC-90	32MBits	Under Testing
MXIC	MX29LV320BTTC-70	32MBits	Under Testing
MXIC	MX29LV320BTTC-90	32MBits	Under Testing
MXIC	MX29LV320BTC-70	32MBits	Under Testing
MXIC	MX29LV320BTC-90	32MBits	Under Testing
MXIC	MX29LV320TTC-70	32MBits	Under Testing
MXIC	MX29LV320TTC-90	32MBits	Under Testing
Winbond	W19B320ABT7H	32MBits	Under Testing
ST	M29W320DT-90	32MBits	Under Testing
ST	M29W320DT-70	32MBits	Under Testing
ST	M29W320DB-70	32MBits	Under Testing
Spansion	S29GL032-90T	32MBits	Under Testing

10. MT537x DDR/2 Supported

Brand	IC Order Number	DDR Type	Description
Nanya	NT5DS32M16BT-5T	DDR	32Mx16, Under Testing
ProMOS	V58C2512164SB5	DDR	32Mx16, Under Testing
Infineon	HYB25DC512160CE–5	DDR	32Mx16, Under Testing
Hynix	HY5DU121622ALT-D43	DDR	32Mx16, Under Testing
MIRA	P2S12D40CTP-G5	DDR	32Mx16, Under Testing
Micron	MT46V32M16TG-5B	DDR	32Mx16, Under Testing
PSC	A2S56D40CTP-G5	DDR	16Mx16, Under Testing
Nanya	NT5DS16M16CS-5T	DDR	16Mx16, Under Testing
ProMOS	V58C2256164SCI5	DDR	16Mx16, Under Testing
Hynix	HY5DU561622CT-5	DDR	16Mx16, Under Testing

Specifications are subject to change without notice

ELPIDA	DD2516AKTA-6B-E	DDR	16Mx16, Under Testing
Infineon	HYB25DC256160CE-5	DDR	16Mx16, Under Testing
MIRA	P2S56D40CTP-G5	DDR	16Mx16, Under Testing
Micron	MT46V16M16TG-5B	DDR	16Mx16, Under Testing
Samsung	K4D551638F-LC50	GDDR	16Mx16, Under Testing
PSC	A3R12E4FDF-G6EA	DDR2	32Mx16, Under Testing
Infinion	HYB18TC512160AF-3S	DDR2	32Mx16, Under Testing
ProMOS	*V59C1512164QA*-3	DDR2	32Mx16, Under Testing
Nanya	NT5TU32M16AG-3C	DDR2	32Mx16, Under Testing
Hynix	HY5PS121621LF-Y5	DDR2	32Mx16, Under Testing
Micron	MT47H32M16-3	DDR2	32Mx16, Under Testing
Infinion	HYB18TC256160AF-3S	DDR2	16Mx16, Under Testing
Hynix	HY5PS561621LF-Y5	DDR2	16Mx16, Under Testing
Micron	MT47H16M16-3	DDR2	16Mx16, Under Testing

11. MT537x PCB Layout Guidelines

- 4-layer PCB Design (TOP / GND / POWER / BOTTOM)
- Power Arrangement
  1. DV33 : Supply to MT537x Digital and Peripheral
  2. AV33 : Supply to MT537x Analog
  3. DV25/DV18 : Supply to MT537x and DDR/2
  4. AV15 : Supply to MT537x Video Front-end 1 (YPbPr/RGB)
  5. AV15_DAC : Supply to MT537x Video DAC
  6. DV12 : Supply to MT537x Digital
  7. AV12 : Supply to MT537x Analog
- Power Plane
  1. The Power has High Priority in Layer 3
  2. If There are No Enough Plane in Layer 3, the Power Line Should be Routed Wider (Component Side Has High Priority)
  3. Be Care the Power Return Path, Especially for Large Power
  4. The Switching Power Should leave alone the Analog Portion
- Ground Plane
  1. In General, We Use Only One Ground (Don't Divided) in Layer 2
  2. You May Have Independent Ground if There are Large Power Consumption in Your Design, for Example - Digital Audio AMP. But You Should Note That the

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Signal Return Path

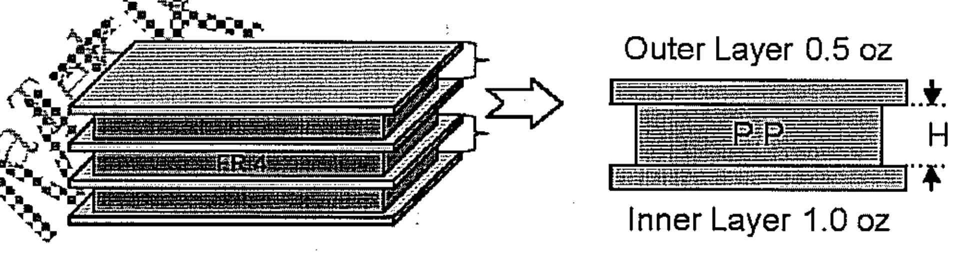
3. Please Flush the Copper both in Component and Solder Sides

- The Bypass Cap. Should be Located as Close to IC's Power Pin as Possible
- The VCXO or Crystal Should be Located as Close to IC as Possible
- The Video Termination Resistor Should be Closed to Connector
- The Video AC-couple Cap. Should be Closed to MT537x
- Video Signal YPbPr and RGB Don't Cross with Other Signal (Must)
- Video Signal CVBS and S-Video Don't Cross with Other Signal as Possible. If Need, Please Add Ground Shielding (Guard Trace) on the Side of the Video
- Audio Signal (Analog) Don't Cross with Other Signal as Possible. If Need, Please Add Ground Shielding (Guard Trace) on the Side of the Audio
- To Avoid Routing any Traces on the Ground or Power Plane
- Digital Signal Width Please Use 6 mil
- DDR/2 Layout – Please Follow the Layout Guide Described Below or Copy from MTK's Library to Speed-up the Design Time
  If You had Re-layout the DDR/2, Please Provide the Layout File for DDR/2 SI Simulation (Familiar with PowerPCB Format)
- HDMI / LVDS Layout – Please Follow the Layout Guide Described Below

12. MT537x DDR/2 Layout Guide

12.1 4 Layer PCB Layout Constraints

12.1.1 Board Stack-up



PCB Stackup – 4 Layers

Specifications are subject to change without notice

The outer layers of the PCB were designated to the mainly signal routings by default, and normally were chosen to have the 0.5 oz Cu foil with plated 0.5 oz copper, and the inner layers was designated to be 1.0 oz at the PCB manufacturing step.

The dielectrics between conductors were as the isolators, which were used to separate the conductors. By the micro-strip line architecture of system memory signals, the target impedance was desired to have 55Ω +/- 10%. Please refer to the table below for your PCB design and recommendation. The default design was 6 mil trace width with 4.5 mil height dielectrics.

4 Layer PCB Stack-up Configurations

PCB Parameter			
Trace Width (mil)	H (mil)	Target Impedance (Ω)	Tolerance
5	4.5	56	10%

Please request the PCB manufactory to follow the FR4 stack-up as below

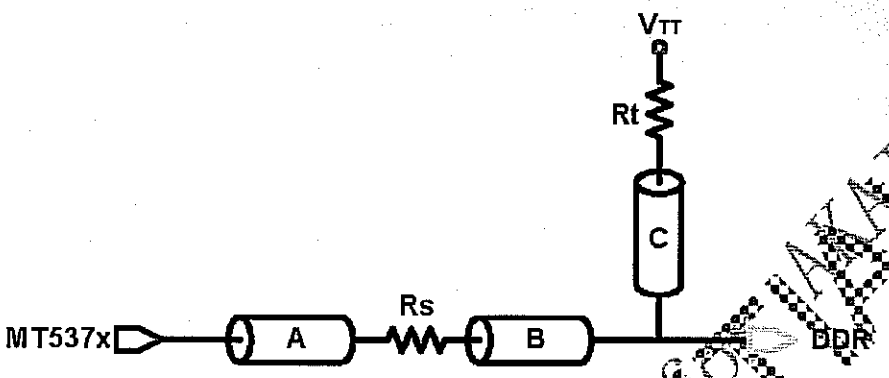
Description	Material	Height (mil)	PS
Conductor		0.5 oz	
Medium	☐ No Assigned ☒ Assigned	4.5	2116
Conductor		1 oz	
Medium		47.6	
Conductor		1 oz	
Medium		4.5	
Conductor		0.5 oz	

12.2 System DDR Memory Solution Space

Refer to the diagrams below to the topologies of the DDR signals, and the actual dimension specifications were listed of the tables

12.2.1 DDR Signal Topology – 1 (DS / DQS / DQM)

Specifications are subject to change without notice



DDR Signal Topology - 1

Signal			DQ	DQS	DQM
Trace (mil)	Width (W)		5	5	5
	Spacing		8 or Above	8 or Above	8 or Above
Trace Length (inch)	A	Min.	0.2	0.2	0.2
		Max.	1	1	1
	B	Min.	0.2	0.2	0.2
		Max.	1.2	1.2	1.2
	C	Min.	0.1	0.1	0.1
		Max.	0.5	0.5	0.5
	A+B	Min.	0.4	0.4	0.4
		Max.	2	2	2
Rs (Ω)			47	47	47
Rt (Ω)			75	75	75

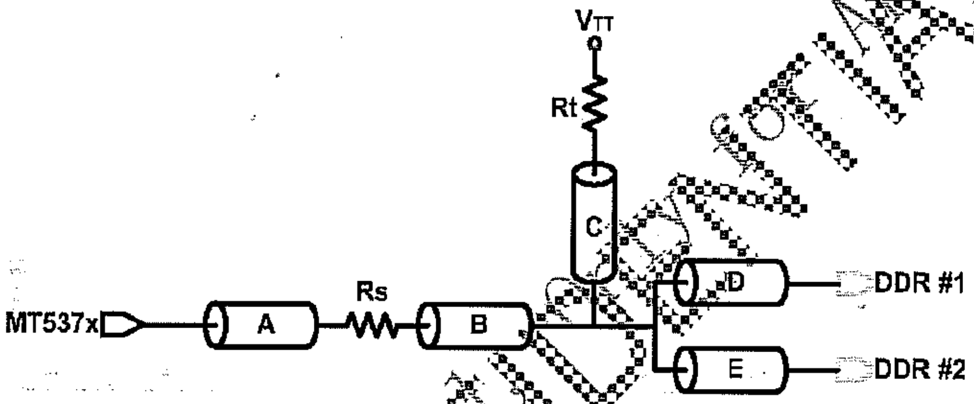
Note :

1. Keep the difference of the trace length of the same data signal groups within about 200 mils as possible.
2. Keep the difference of the data signal groups within 200 mils as possible (The longest signal trace to the shortest signal trace).
3. Placing the damping resistor close to the MT537x.
4. Placing the termination resistor close to the memory as possible.
5. Put an integrated plane as the return path to the signals beneath the data signals.
6. When the signal need to change layers, and the reference paths beneath

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the signal are not continued, placing the bypass capacitors nearing to the vias where are the points to change layers and connecting the capacitors to the different reference paths.

12.2.2 DDR Signal Topology – 2 (Address and Command)



DDR Signal Topology - 2

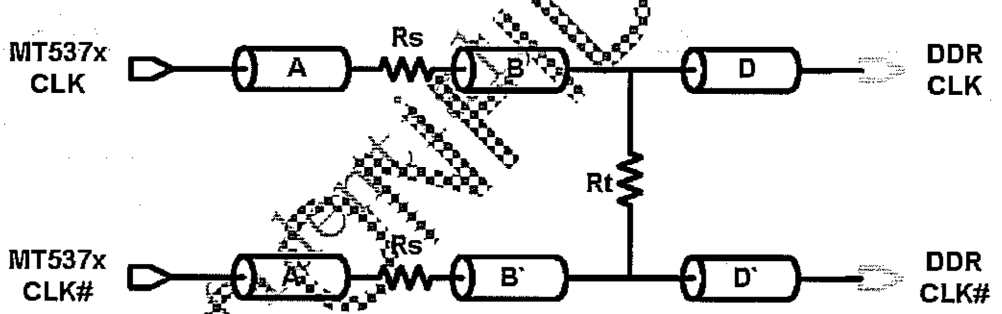
Signal			RA / BA	CS# / CAS# / RAS# / WE#	CKE
Trace (mil)		Width (W)	5	5	5
		Spacing	8 or Above	8 or Above	8 or Above
Trace Length (inch)	A	Min.	0.2	0.2	0.2
		Max.	1.2	1.2	1.2
	B	Min.	0.2	0.2	0.2
		Max.	2	2	2
	C	Min.	0	0	0
		Max.	0.5	0.5	0.5
	D / E	Min.	0.2	0.2	0.2
		Max.	1.2	1.2	1.2
	A+B+D (or E)	Min.	0.6	0.6	0.6
		Max.	4.2	4.2	4.2
Rs (Ω)			22	22	22
Rt (Ω)			75	75	75

Specifications are subject to change without notice

Note :

1. Keep the difference of the branches' length (D / E) of the dual loads signal within 100 mils.
2. Placing the damping resistor close to the MT537x.
3. Put the termination resistor close to the crossing point of the branches.
4. Reserving more spacing to the periodic signal (as clock) if signal was critical and there weren't the guard traces.
5. Put an integrated plane as the return path to the signals beneath the address / command signals.
6. When the signal need to change layers, and the reference paths beneath the signal are not continued, placing the bypass capacitors nearing to the vias where are the points to change layers and connecting the capacitors to the different reference paths.

12.2.3 DDR Signal Topology – 3 (Clock Pair)



DDR Signal Topology - 3

Signal			CLK / CLK#
Trace (mil)		Width	5
		Spacing	8 or Above
Trace Length (inch)	A	Min.	0.2
		Max.	1
	B	Min.	0.2
		Max.	1
	D	Min.	0.2
		Max.	1.2
	A+B+D	Min.	0.6

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		Max.	2.6
Rs (Ω)			47
Rt (Ω)			100

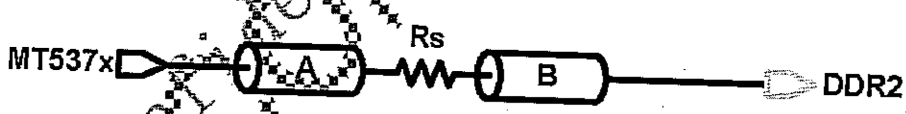
Note :

1. The trace length of A / A`, B / B`, D / D` should be as equal as possible.
2. Keep the trace difference between CLK / CLK# in +/- 100 mils.
3. Keep the trace difference between DQ / DQS / DQM and CLK in +/- 200 mils.
4. Keep the trace difference between RA / BA / CS# / CAS# / RAS# / WE# / CKE and CLK in +/- 1000 mils.

12.3 System DDR2 Memory Solution Space

Refer to the diagrams below to the topologies of the DDR2 signals, and the actual dimension specifications were listed of the tables.

12.3.1 DDR2 Signal Topology – 1 (DQ and DQM)



DDR2 Signal Topology - 1

Signal			DQ	DQM
Trace (mil)		Width (W)	5	5
		Spacing	8 or Above	8 or Above
Lengt	A	Min.	0.2	0.2
		Max.	1	1
	B	Min.	0.2	0.2

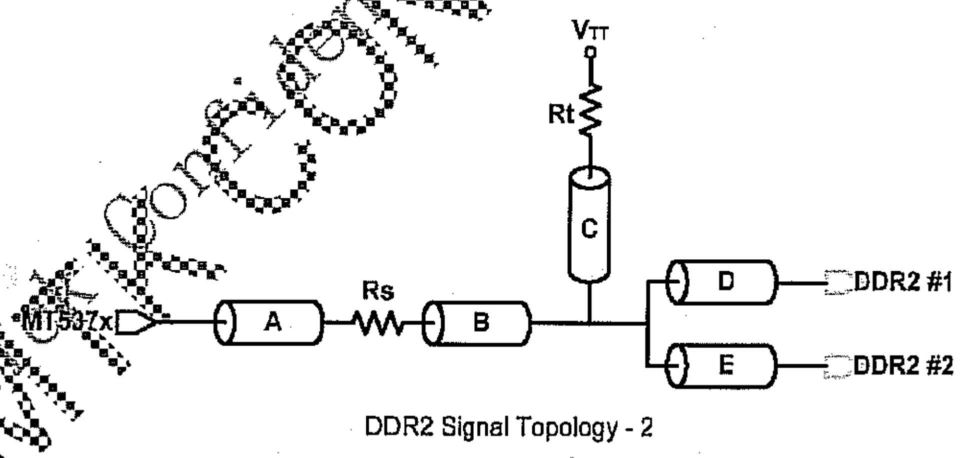
Specifications are subject to change without notice

		Max.	1.2	1.2
	A+B	Min.	0.4	0.4
		Max.	2	2
Rs (Ω)			22	22

Note :

1. Keep the difference of the trace length of the same data signal groups within about 200 mils as possible.
2. Keep the difference of the data signal groups within 200 mils as possible (The longest signal trace to the shortest signal trace).
3. Placing the damping resistor close to the MT537x.
4. Placing the termination resistor close to the memory as possible.
5. Put an integrated plane as the return path to the signals beneath the data signals.
6. When the signal need to change layers and the reference paths beneath the signal are not continued, placing the bypass capacitors nearing to the vias where are the points to change layers and connecting the capacitors to the different reference paths.

12.3.2 DDR2 Signal Topology – 2 (Address and Command)



DDR2 Signal Topology - 2

Signal		RA / BA	CS# / CAS# / RAS# / WE#	CKE
Trace (mil)	Width (W)	5	5	5

Specifications are subject to change without notice

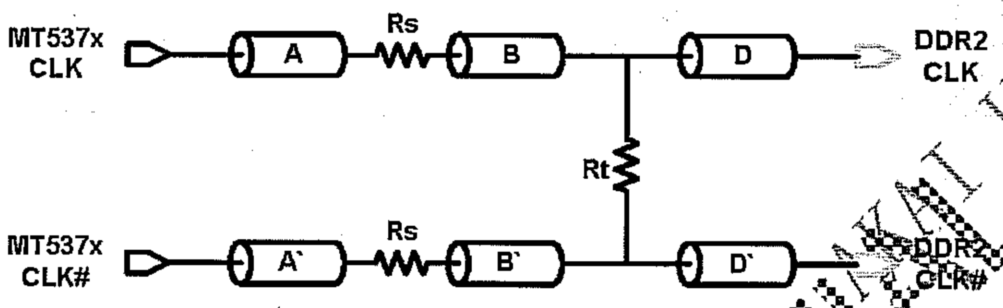
		Spacing	8 or Above	8 or Above	8 or Above
Trace Length (inch)	A	Min.	0.2	0.2	0.2
		Max.	1.2	1.2	1.2
	B	Min.	0.2	0.2	0.2
		Max.	2	2	2
	C	Min.	0	0	0
		Max.	0.5	0.5	0.5
	D / E	Min.	0.2	0.2	0.2
		Max.	1.2	1.2	1.2
	A+B+D (or E)	Min.	0.6	0.6	0.6
		Max.	4.2	4.2	4.2
Rs (Ω)			22	22	22
Rt (Ω)			75	75	75

Note :

1. Keep the difference of the branches length (D / E) of the dual loads signal within 100 mils.
2. Placing the damping resistor close to the MT537x.
3. Put the termination resistor close to the crossing point of the branches.
4. Reserving more spacing to the periodic signal (as clock) if signal was critical and there weren't the guard traces.
5. Put an integrated plane as the return path to the signals beneath the address / command signals.
6. When the signals need to change layers, and the reference paths beneath the signal are not continued, placing the bypass capacitors nearing to the vias where are the points to change layers and connecting the capacitors to the different reference paths.

12.3.3 DDR2 Signal Topology – 3 (Clock and DQS)

Specifications are subject to change without notice



DDR2 Signal Topology - 3

Signal			CLK / CLK#	DQS / DQS#
Trace (mil)		Width (W)	5	5
		Spacing	8 or Above	8 or Above
Trace Length (inch)	A	Min.	0.2	0.2
		Max.	1	1
	B	Min.	0.2	0.2
		Max.	1	1
	D	Min.	0.1	NS
		Max.	1.2	NS
	A+B+D	Min.	0.6	0.4
		Max.	2.6	2
Rs (Ω)			22	22
Rt (Ω)			100	NS

Note :

1. The trace length of A / A`, B / B`, D / D` should be as equal as possible.
2. Keep the trace difference between CLK / CLK# in +/- 100 mils.
3. Keep the trace difference between DQ / DQS / DQM and CLK in +/- 200 mils.
4. Keep the trace difference between RA / BA / CS# / CAS# / RAS# / WE# / CKE and CLK in +/- 1000 mils.

13. MT537x HDMI / LVDS Layout Guide

13.1 HDMI / LVDS Signal PCB Layout Guideline

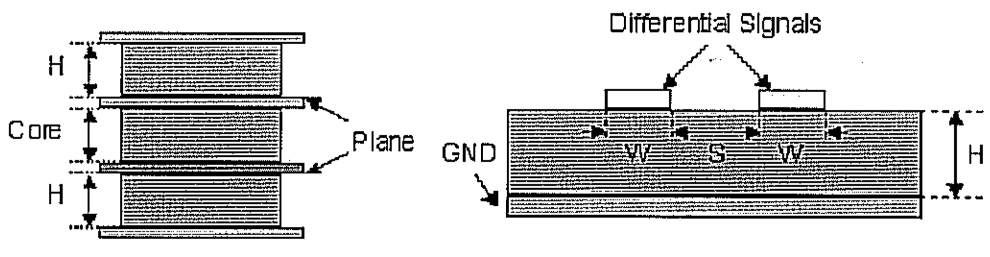
Specifications are subject to change without notice

For the other applications of the high-speed signal PCB design, below illustrated the topologies and constraints of the HDMI / LVDS or other differential signals that were achieved to the electrical requirements. Also refer to the form to the detail recommendations.

13.2 Multi-Layer PCB Design

By the default multi-layers PCB architecture, the inner layers were assigned to be the reference plane to the signals. For the signal integrity issues, the integrate plane would held to hold a good signal qualities when signal were proceeding on the signal traces. Refer to the below shown the stack up and the topology of the differential signals of the 4-layer PCB where the signals were routed of the outer layers.

13.2.1 Signals without Guard Traces



HDMI / LVDS Signal Topology - 4 Layer

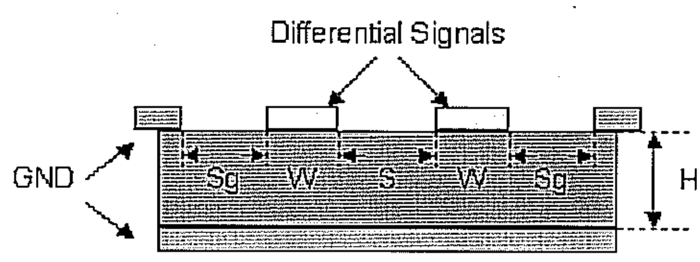
Variable	Nominal (mil)	Tolerance	Min. (mil)	Max. (mil)
Trace High (H)	4.5 (2116)			
Trace Width (W)	5	+ / - 1 mil	4	6
Spacing (S)	8 (mil)	+ / - 1 mil	9	7
Single Ended Trace Impedance	56Ω		61.6Ω	52.6Ω
Differential Trace Impedance	98Ω		109Ω	89.9Ω
Reference Plane	Ground	Ground	Ground	Ground

13.2.2 Signals with Guard Traces

The other application was used the coplanar ground copper and surrounded the

Specifications are subject to change without notice

signals to achieve the noise shielding purpose. The figure shows the signal topology.

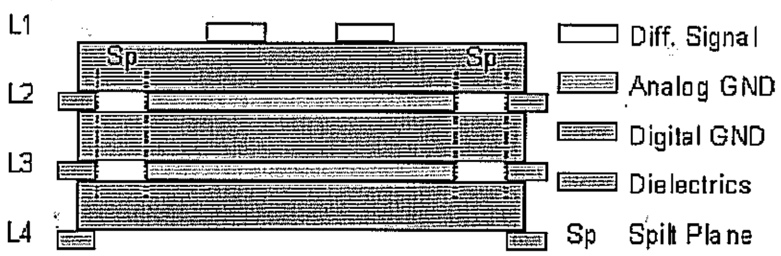


Differential Signal with Guard Trace

Variable	Nominal (mil)	Tolerance	Min. (mil)	Max. (mil)
Trace High (H)	4.5 (2116)			
Trace Width (W)	5	+ / - 1 mil	4	6
Spacing (S)	8 (mil)	+ / - 1 mil	9	7
Spacing to GND(Sg)	8 (mil)	+ / - 1 mil	9	7
Single Ended Trace Impedance	55Ω		60Ω	50.5Ω
Differential Trace Impedance	97Ω		107Ω	87Ω
Reference Plane	Ground	Ground	Ground	Ground

Note:

1. Keeping the spacing to the other signals as far as possible.
2. Keeping the spacing to different ground planes (Sp) more than 30 mils as possible as the below.



Cross-Section of Plane Designated

Specifications are subject to change without notice

14. MT537x BGA Soldering Information

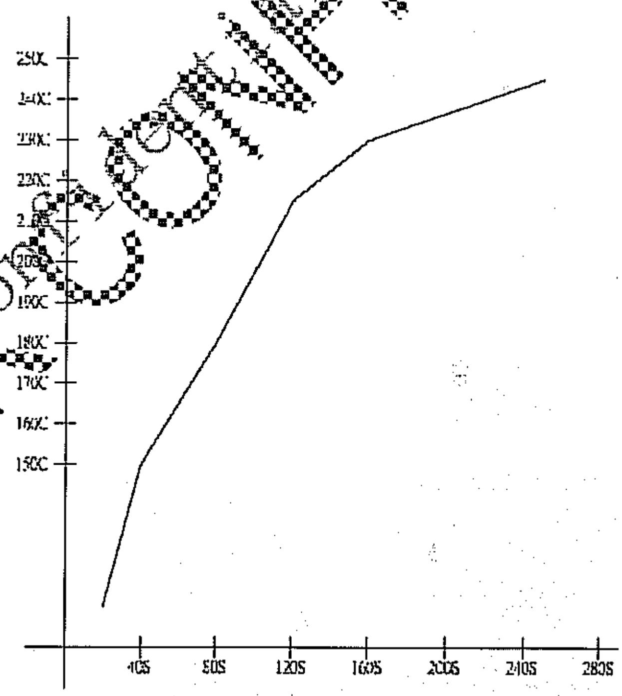
14.1 MT537xAG is Lead-Free Process

Element :

1. Sn : 95.5 %
2. Ag : 4 %
3. Cu : 0.3 %
4. Fusion Point : 228 °C.

14.2 Soldering Control (for Reference Only)

1. 150 °C : 40 Sec
2. 180 °C : 40 Sec
3. 215 °C : 40 Sec
4. 230 °C : 40 Sec
5. 245 °C : 90 Sec
6. 245 °C : 30 Sec



Specifications are subject to change without notice

15. US Terrestrial TV Channel Frequencies

US Terrestrial TV Channel Frequencies					
Channel	TV Video Freq (MHz)	ATSC Center Freq (MHz)	Channel	Video Freq (MHz)	ATSC Center Freq (MHz)
2	55.25	57	36	603.25	605
3	61.25	63	37	609.25	611
4	67.25	69	38	615.25	617
5	77.25	79	39	621.25	623
6	83.25	85	40	627.25	629
7	175.25	177	41	633.25	635
8	181.25	183	42	639.25	641
9	187.25	189	43	645.25	647
10	193.25	195	44	651.25	653
11	199.25	201	45	657.25	659
12	205.25	207	46	663.25	665
13	211.25	213	47	669.25	671
14	471.25	473	48	675.25	677
15	477.25	479	49	681.25	683
16	483.25	485	50	687.25	689
17	489.25	491	51	693.25	695
18	495.25	497	52	699.25	701
19	501.25	503	53	705.25	707
20	507.25	509	54	711.25	713
21	513.25	515	55	717.25	719
22	519.25	521	56	723.25	725
23	525.25	527	57	729.25	731
24	531.25	533	58	735.25	737
25	537.25	539	59	741.25	743
26	543.25	545	60	747.25	749
27	549.25	551	61	753.25	755

Specifications are subject to change without notice

28	555.25	557	62	759.25	761
29	561.25	563	63	765.25	767
30	567.25	569	64	771.25	773
31	573.25	575	65	777.25	779
32	579.25	581	66	783.25	785
33	585.25	587	67	789.25	791
34	591.25	593	68	795.25	797
35	597.25	599	69	801.25	803

16. US Cable TV Channel Frequencies

16.1 Standard TV Channel

US Cable TV STD Channel Frequencies					
Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)	Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)
2	55.25	57	64	463.25	465
3	61.25	63	65	469.25	471
4	67.25	69	66	475.25	477
1	—	—	67	481.25	483
5	77.25	79	68	487.25	489
6	83.25	85	69	493.25	495
95	91.25	93	70	499.25	501
96	97.25	99	71	505.25	507
97	103.25	105	72	511.25	513
98	109.25	111	73	517.25	519
99	115.25	117	74	523.25	525
14	121.25	123	75	529.25	531
15	127.25	129	76	535.25	537
16	133.25	135	77	541.25	543
17	139.25	141	78	547.25	549
18	145.25	147	79	553.25	555
19	151.25	153	80	559.25	561

Specifications are subject to change without notice

20	157.25	159	81	565.25	567
21	163.25	165	82	571.25	573
22	169.25	171	83	577.25	579
7	175.25	177	84	583.25	585
8	181.25	183	85	589.25	591
9	187.25	189	86	595.25	597
10	193.25	195	87	601.25	603
11	199.25	201	88	607.25	609
12	205.25	207	89	613.25	615
13	211.25	213	90	619.25	621
23	217.25	219	91	625.25	627
24	223.25	225	92	631.25	633
25	229.25	231	93	637.25	639
26	235.25	237	94	643.25	645
27	241.25	243	100	649.25	651
28	247.25	249	101	655.25	657
29	253.25	255	102	661.25	663
30	259.25	261	103	667.25	669
31	265.25	267	104	673.25	675
32	271.25	273	105	679.25	681
33	277.25	279	106	685.25	687
34	283.25	285	107	691.25	693
35	289.25	291	108	697.25	699
36	295.25	297	109	703.25	705
37	301.25	303	110	709.25	711
38	307.25	309	111	715.25	717
39	313.25	315	112	721.25	723
40	319.25	321	113	727.25	729
41	325.25	327	114	733.25	735
42	331.25	333	115	739.25	741
43	337.25	339	116	745.25	747
44	343.25	345	117	751.25	753
45	349.25	351	118	757.25	759
46	355.25	357	119	763.25	765
47	361.25	363	120	769.25	771
48	367.25	369	121	775.25	777
49	373.25	375	122	781.25	783

50	379.25	381	123	787.25	789
51	385.25	387	124	793.25	795
52	391.25	393	125	799.25	801
53	397.25	399	126	805.25	807
54	403.25	405	127	811.25	813
55	409.25	411	128	817.25	819
56	415.25	417	129	823.25	825
57	421.25	423	130	829.25	831
58	427.25	429	131	835.25	837
59	433.25	435	132	841.25	843
60	439.25	441	133	847.25	849
61	445.25	447	134	853.25	855
62	451.25	453	135	859.25	861
63	457.25	459			

16.2 IRC TV Channel

US Cable TV IRC Channel Frequencies					
Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)	Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)
2	55.25	57	64	463.25	465
3	61.25	63	65	469.25	471
4	67.25	69	66	475.25	477
1	73.25	75	67	481.25	483
5	79.25	81	68	487.25	489
6	85.25	87	69	493.25	495
95	91.25	93	70	499.25	501
96	97.25	99	71	505.25	507
97	103.25	105	72	511.25	513
98	–	–	73	517.25	519
99	–	–	74	523.25	525
14	121.15	122.9	75	529.25	531

Specifications are subject to change without notice

15	127.15	128.9	76	535.25	537
16	133.15	134.9	77	541.25	543
17	139.15	140.9	78	547.25	549
18	145.15	146.9	79	553.25	555
19	151.15	152.9	80	559.25	561
20	157.15	158.9	81	565.25	567
21	163.15	164.9	82	571.25	573
22	169.15	170.9	83	577.25	579
7	175.25	177	84	583.25	585
8	181.25	183	85	589.25	591
9	187.25	189	86	595.25	597
10	193.25	195	87	601.25	603
11	199.25	201	88	607.25	609
12	205.25	207	89	613.25	615
13	211.25	213	90	619.25	621
23	217.25	219	91	625.25	627
24	223.25	225	92	631.25	633
25	229.25	231	93	637.25	639
26	235.25	237	94	643.25	645
27	241.25	243	100	649.25	651
28	247.25	249	101	655.25	657
29	253.25	255	102	661.25	663
30	259.25	261	103	667.25	669
31	265.25	267	104	673.25	675
32	271.25	273	105	679.25	681
33	277.25	279	106	685.25	687
34	283.25	285	107	691.25	693
35	289.25	291	108	697.25	699
36	295.25	297	109	703.25	705
37	301.25	303	110	709.25	711
38	307.25	309	111	715.25	717
39	313.25	315	112	721.25	723
40	319.25	321	113	727.25	729
41	325.25	327	114	733.25	735

Specifications are subject to change without notice

42	--	--	115	739.25	741
43	337.25	339	116	745.25	747
44	343.25	345	117	751.25	753
45	349.25	351	118	757.25	759
46	355.25	357	119	763.25	765
47	361.25	363	120	769.25	771
48	367.25	369	121	775.25	777
49	373.25	375	122	781.25	783
50	379.25	381	123	787.25	789
51	385.25	387	124	793.25	795
52	391.25	393	125	799.25	801
53	397.25	399	126	805.25	807
54	403.25	405	127	811.25	813
55	409.25	411	128	817.25	819
56	415.25	417	129	823.25	825
57	421.25	423	130	829.25	831
58	427.25	429	131	835.25	837
59	433.25	435	132	841.25	843
60	439.25	441	133	847.25	849
61	445.25	447	134	853.25	855
62	451.25	453	135	859.25	861
63	457.25	459			

16.3 HRC TV Channel

US Cable TV HRC Channel Frequencies					
Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)	Channel	TV Video Freq (MHz)	QAM Center Freq (MHz)
2	54	55.75	64	462	463.75
3	60	61.75	65	468	469.75

Specifications are subject to change without notice

4	66	67.75	66	474	475.75
1	72	73.75	67	480	481.75
5	78	79.75	68	486	487.75
6	84	85.75	69	492	493.75
95	90	91.75	70	498	499.75
96	96	97.75	71	504	505.75
97	102	103.75	72	510	511.75
98	–	–	73	516	517.75
99	–	–	74	522	523.75
14	120	121.75	75	528	529.75
15	126	127.75	76	534	535.75
16	132	133.75	77	540	541.75
17	138	139.75	78	546	547.75
18	144	145.75	79	552	553.75
19	150	151.75	80	558	559.75
20	156	157.75	81	564	565.75
21	162	163.75	82	570	571.75
22	168	169.75	83	576	577.75
7	174	175.75	84	582	583.75
8	180	181.75	85	588	589.75
9	186	187.75	86	594	595.75
10	192	193.75	87	600	601.75
11	198	199.75	88	606	607.75
12	204	205.75	89	612	613.75
13	210	211.75	90	618	619.75
23	216	217.75	91	624	625.75
24	222	223.75	92	630	631.75
25	228	229.75	93	636	637.75
26	234	235.75	94	642	643.75
27	240	241.75	100	648	649.75
28	246	247.75	101	654	655.75
29	252	253.75	102	660	661.75
30	258	259.75	103	666	667.75
31	264	265.75	104	672	673.75

Specifications are subject to change without notice

32	270	271.75	105	678	679.75
33	276	277.75	106	684	685.75
34	282	283.75	107	690	691.75
35	288	289.75	108	696	697.75
36	294	295.75	109	702	703.75
37	300	301.75	110	708	709.75
38	306	307.75	111	714	715.75
39	312	313.75	112	720	721.75
40	318	319.75	113	726	727.75
41	324	325.75	114	732	733.75
42	330	331.75	115	738	739.75
43	336	337.75	116	744	745.75
44	342	343.75	117	750	751.75
45	348	349.75	118	756	757.75
46	354	355.75	119	762	763.75
47	360	361.75	120	768	769.75
48	366	367.75	121	774	775.75
49	372	373.75	122	780	781.75
50	378	379.75	123	786	787.75
51	384	385.75	124	792	793.75
52	390	391.75	125	798	799.75
53	396	397.75	126	804	805.75
54	402	403.75	127	810	811.75
55	408	409.75	128	816	817.75
56	414	415.75	129	822	823.75
57	420	421.75	130	828	829.75
58	426	427.75	131	834	835.75
59	432	433.75	132	840	841.75
60	438	439.75	133	846	847.75
61	444	445.75	134	852	853.75
62	450	451.75	135	858	859.75
63	456	457.75			

MT5112BD
Preliminary Datasheet

- FEATURES
- GENERAL DESCRIPTION
- FUNCTIONAL BLOCK DIAGRAM
- PIN ASSIGNMENT
- PIN DESCRIPTION
- TIMING INFORMATION
- ELECTRICAL CHARACTERISTICS
- OUTLINE DIMENSION & TOP MARKING

FEATURES

- Compliant with ATSC digital television standard
- Supports SCTE DVS-031 and ITU J.83 Annex B digital CATV standard
- Accepts direct IF (44 MHz or 43.75MHz) and low IF (5.38MHz)
- Differential IF input with programmable input signal level: 0.5Vpp to 2Vpp
- NTSC interference rejection capability
- Compensate echo up to -35 to +60*us* range for terrestrial HDTV reception
- Pass all Brazil fading channel ensembles
- Meet all ATSC/A74 requirement
- On-chip programmable gain amplifier
- 25MHz crystal for clock generation
- Excellent adjacent and co-channel rejection capability, only single SAW is required
- Full-digital timing recovery, no VCXO is required
- Full-digital frequency offset recovery with wide acquisition range ±1MHz for ATSC and ±250kHz for CATV reception
- Dual digital AGC controls for IF and RF respectively
- MPEG-2 transport stream output in parallel or serial format
- On-chip error rate estimators for TS packets, TCM decoder, and equalizer
- EIA/CEA-909 antenna interface, both mode A and mode B are supported
- Controlled by I^2C interface
- Supports sleep mode to save power consumption
- Core power supply: 1.8V, peripheral power supply: 3.3V
- 100-TQFP with lead free package

GENERAL DESCRIPTION

The MT5112BD is a highly integrated single-chip for digital terrestrial HDTV and digital cable TV demodulation. The chip is designed specifically for the digital terrestrial HDTV and CATV receivers, and is fully compliant with ATSC A/53, SCTE DVS-031, and ITU J.83 Annex B standards.

DTV

8-VSB and Clear-QAM Reception

MT5112BD contains a 10-bit A/D converter, an 8-VSB/QAM demodulator, followed by a trellis-coded modulation (TCM) decoder and a Reed-Solomon forward error correction (FEC) decoder. Moreover, an embedded 8-bit microprocessor intelligently handles the acquisition and tracking to ensure the best receiving performance under various channel conditions. The microprocessor communicates with the external host controller via an I^{2}C-compatible interface, and also provides direct control to the RF tuner via another I^{2}C-compatible interface.

MT5112BD accepts the tuner IF output centered at 44MHz or 43.75MHz, or the low IF signals from a down-converter. With good adjacent channel immunity, additional IF SAW filters for adjacent channel rejection can be saved. An on-chip programmable gain-controlled amplifier (PGA) is designed to provide extra signal gain when the tuner output level is low. The amplified IF signal is then sample and digitized for further demodulation process.

MT5112BD keeps A/D input power level at a desired level so as to maximize the received SNR. It measures the power level of the digitized samples and provide two signals (both sigma-delta encoded; one delayed and one non-delayed) for front-end gain control purpose. The signals is low-pass filtered before connected to tuner or IF gain stages.

For the 8-VSB reception, the carrier frequency offset is estimated and compensated by a fully digital synchronizer. It also controls the rate conversion in the digital re-sampling device by estimating the sampling frequency offset; hence no external VCXO is required. The digital synchronizer simultaneously offers very wide frequency acquisition range and stable tracking capability. This makes MT5112BD robust

work under severe impairment conditions.

The MT5112BD is equipped with a powerful equalizer for mitigating the multi-path effects due to terrestrial propagation of 8-VSB signals. The delicate equalizer design makes the MT5112BD boast its ability for strong echo cancellation. With this powerful equalizer, the MT5112BD can not only easily pass the tests of A74 equalization mask, ATTC channel ensembles, CRC channel ensembles, but also provide superior capability of live signal receptions.

For cable signal reception, the MT5112BD adopts the fully digital modules for timing and carrier synchronization, with no external VCXO required. Specially designed carrier synchronization module enables the MT5112BD passing the OpenCable ATP burst and phase noise tests, while maintaining excellent reception performance under normal reception conditions.

The MT5112BD also utilizes a powerful equalizer for performing channel equalization in cable environments. The MT5112BD equipped with this powerful equalizer can easily pass the SCTE channel tests and offer stable and excellent live signal receptions.

The following FEC decoder corrects most of the errors by the concatenation of the TCM and Reed-Solomon decoders with an in-between de-interleaver. Specifically for the digital cable TV reception, the MT5112BD first detects and aligns de-puncturing timing of the received sequence before TCM decoding. Besides, two synchronization circuits are each inserted before the de-interleaver and after the Reed-Solomon decoder to automatically delineate the FEC frames and transport stream packets respectively. An on-chip error rate estimator can simultaneously monitor the receiving qualities at the three stages: the equalizer output, the TCM decoder, and the transport stream packets. At the last stage, the MT5112BD incorporates a buffer to smooth out the uneven arrival time of transport stream packets. The chip finally outputs the smoothed decoded MPEG-2 transport stream packets in either the serial or parallel transport stream format.

In addition to the demodulation of HDTV signal, MT5112BD provides the capability to remove narrow-band interference such as the co-channel NTSC signal and CW tones which generally exists in

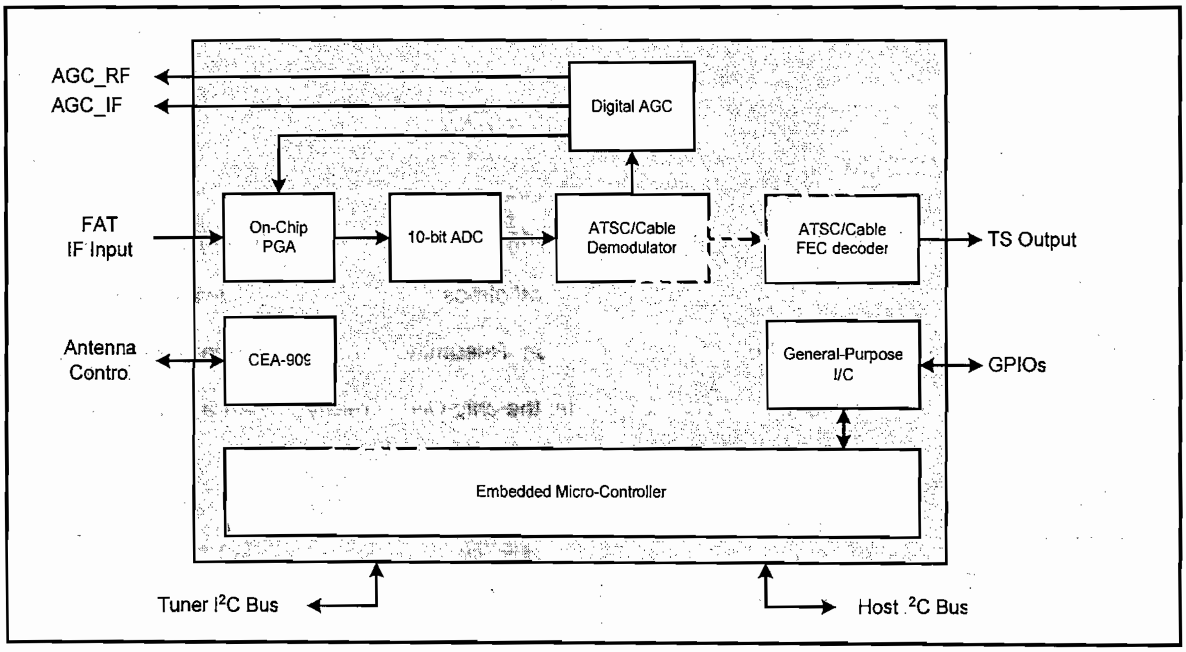
broadcast environment.

To achieve the best reception, an antenna control interface compliant with EIA/CEA-909 is equipped into the MT5112BD to configure the antenna parameters. Both the unidirectional mode A and the bi-directional mode B operation schemes are supported.

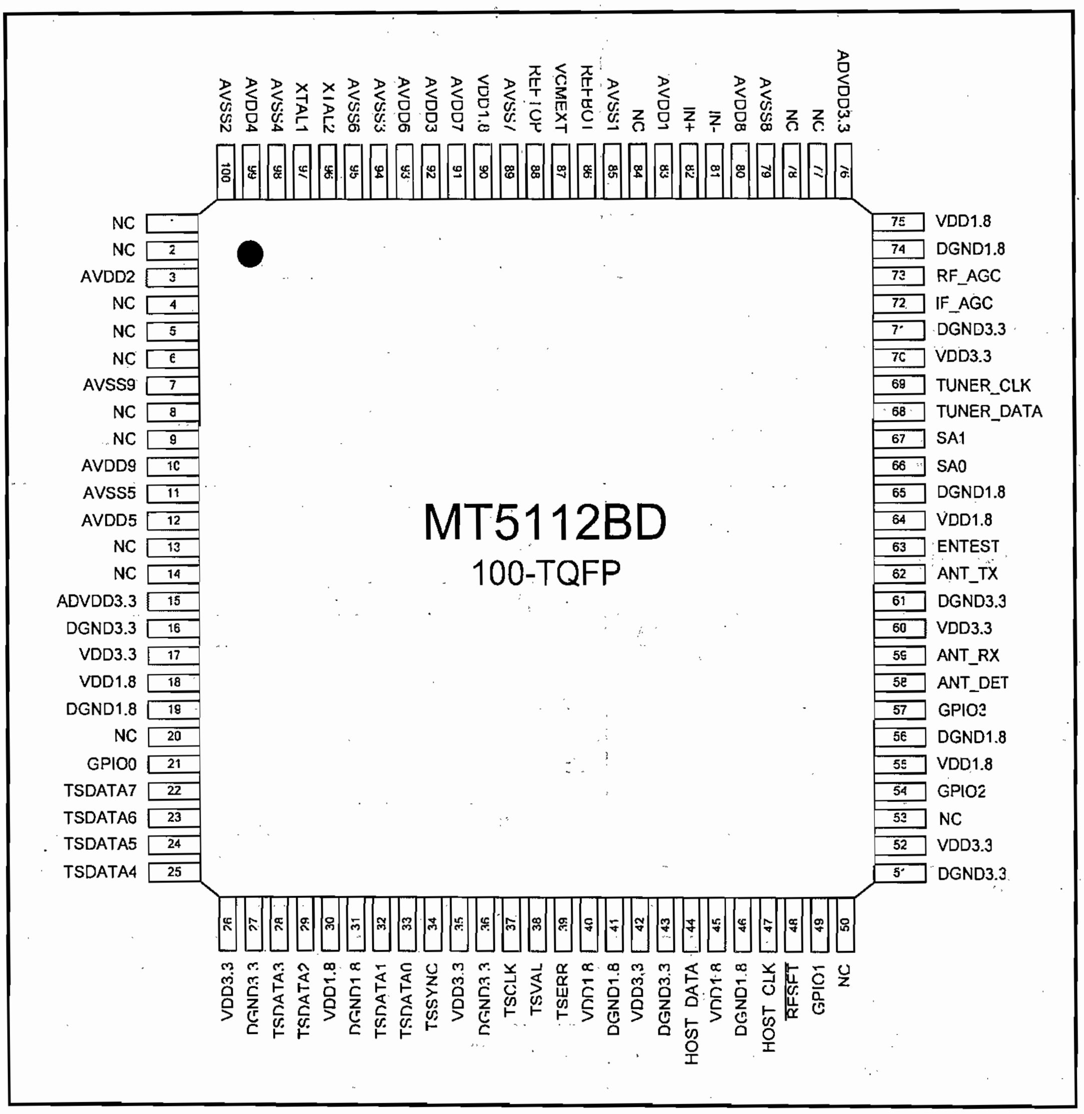
Power Saving Mode

The MT5112BD is designed with efficient mechanisms of power saving. When configured to enter the sleep mode by the system host, it can immediately turn off almost all embedded hardware except the on-chip microprocessor to reduce the power consumption. Resuming from sleep mode is also triggered by the system host. Upon returning to the operation mode, the chip will be ready to start a new acquisition.

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESCRIPTION

For FAT Applications

Pin Numbers	Symbol	Type	Description
Transport Stream			
22, 23, 24, 25, 28, 29, 32, 33	TSDATA[7:0]	O	TS data output
34	TSSYNC	O	TS packet start signal
38	TSVAL	O	TS output valid signal
37	TSCLK	O	TS output clock
39	TSERR	O	TS packet error indicator
Analog Signal			
82	IN+	I	Analog differential IF input
81	IN-	I	
88	REFTOP	O	ADC reference top voltage. Decouple with a capacitor to AVSS
86	REFBOT	O	ADC reference bottom voltage. Decouple with a capacitor to AVSS
87	VCMEXT	O	ADC common mode voltage
Antenna Interface			
62	ANT_TX	O	CEA-909 antenna control: transmit data
58	ANT_DET	I	CEA-909 antenna control: detection signal
59	ANT_RX	I	CEA-909 antenna control: receive data
Clock Generation			
97	XTAL1	I	25MHz crystal input
96	XTAL2	I	
Control Signals			
47	HOST_CLK	I	Host processor serial clock input, 5 volt compatible
44	HOST_DATA	I/O	Host processor serial data pin, 5 volt compatible
69	TUNER_CLK	O	Tuner serial clock output, 5 volt compatible
68	TUNER_DATA	I/O	Tuner serial data pin, 5 volt compatible
72	IF_AGC	O	IF AGC output
73	RF_AGC	O	RF AGC output
48	RESET	I	Power reset pin, low active
66	SA0	I	Chip slave address selection pin, tie to VDD3.3 or DGND
67	SA1	I	Chip slave address selection pin, tie to VDD3.3 or DGND
Power Supply			
17, 26, 35, 42, 52, 60, 70	VDD3.3	P	Digital power supply, tie to 3.3V
18, 30, 40, 45, 55, 64, 75	VDD1.8	P	Digital power supply, tie to 1.8V
16, 19, 27, 31, 36, 41, 43, 46, 51, 56, 61, 63, 65, 71, 74	DGND	P	Digital ground, tie to digital ground plane
3, 10, 12, 80, 83, 91, 92, 93, 99	AVDD	P	Analog power supply, tie to 3.3V
7, 11, 79, 85, 89, 94, 95, 98, 100	AVSS	P	Analog ground, tie to analog ground plane
15, 76	ADVDD3.3	P	Digital power supply for analog component, tie to 3.3V
90	AVDD1.8	P	Digital power supply for analog component, tie to 1.8V
General-Purpose I/O			
57, 54, 49, 21	GPIO[3:0]	I/O	General-Purpose I/Os

Microelectronics

CE2836

24-bit, 192 KHz. CODEC: 6 Ch DAC, 5 Input Mux Stereo ADC

DESCRIPTION

The CE2836 is a mixed signal CMOS monolithic audio Codec. It contains six multi-bit sigma delta DAC and a stereo ADC with 5 input multiplexer, Ideal for audio playback and recording applications.

The DAC consists of 128-time interpolation filters, 3rd order multi-bit ΣΔ modulators, switch capacitors and analog reconstruction filters. The ΣΔ converter offers superior differential linearity, with minimum distortion due to component mis-match. high tolerance to clock jitter. Additionally it includes separated digital volume control for each channel.

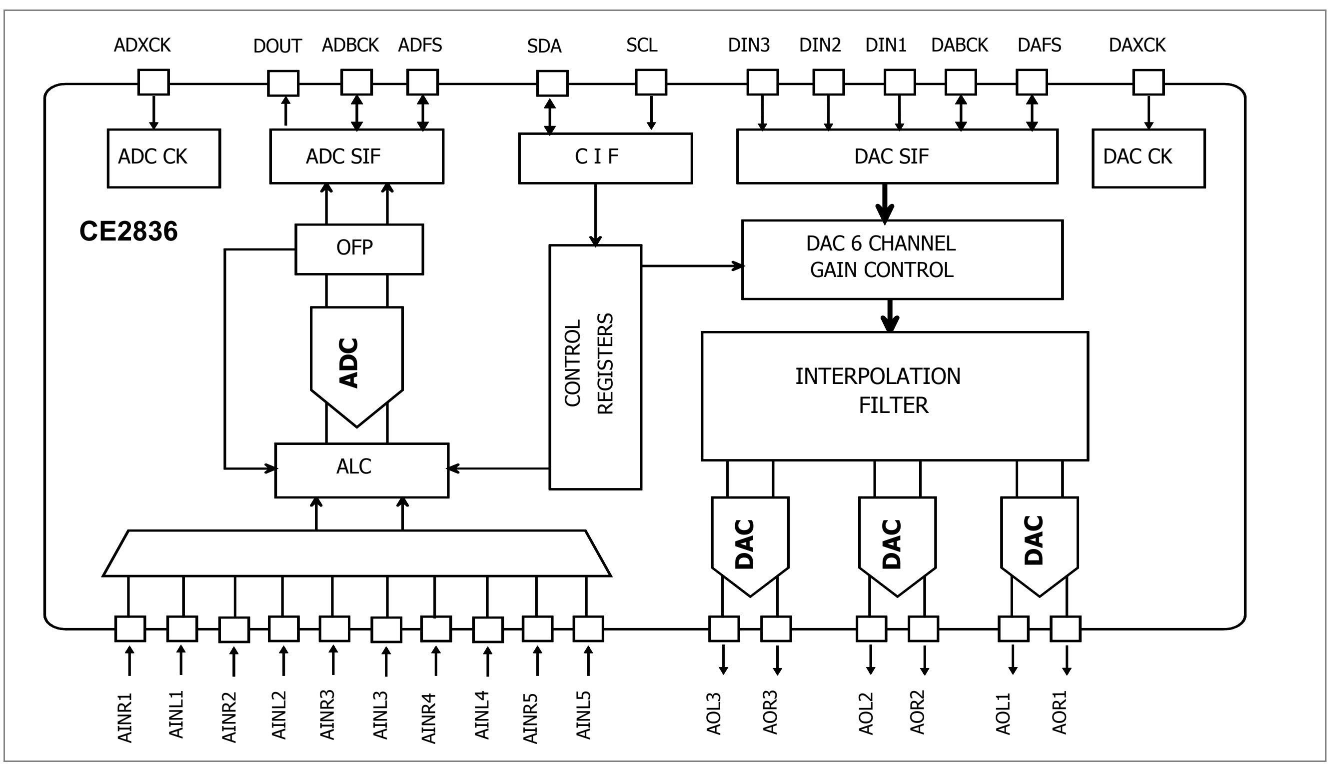
The ADC utilizes cascaded ΣΔ architecture. The internal digital filter has a 20K bandwidth. It support sampling frequency up to 96K Hz. The ADC also includes a analog Automatic Level Control and Noise Gate function to ease the recording applications.

FEATURES

- Six Channel Audio DAC.
  - 104 dB SNR (A Weighted).
  - -82 dB THD + N Ratio (A Weighted).
  - 32K - 192 KHz. Sampling Rates.
  - On -chip Reconstruction Filters.
  - Independent Digital Volume Control.
- Stereo Audio ADC.
  - 5 Channel ADC inputs.
  - Up to 96K Sampling Rate.
  - With Automatic Level Control and Noise Gate.
  - Includes ALC and Noise Gate Functions.
- I^2S, Left and Right Justified Digital I/F Formats.
- 2-wire Serial Control Interface.
- 3.3 Volt Power Supply.

Applications

- Digital Surround Sound For Home Theatre
- DVD or DVD Recordable.



CE2836 Performance

Item	DAC PERFORMANCE SPECIFICATIONS	Spec.
1	Audio Output Level	1 Vrms
2	Audio Bandwidth 20Hz - 20 KHz	+/- 0.1 dB
3	SNR (A-weight)	>104 dB
4	THD + NOISE (A-weight, 0 dB input)	< -82 dB
5	Dynamic Range	94 dB
6	Channel Separation	< -92 dB
7	Nonlinear Distortion	< 0.25 dB
8	Channel Gain Error	< 0.1 dB
	ADC PERFORMANCE SPECIFICATIONS	
1	Maximum Input Level	4 Vpp
2	0 dB Audio Input Level	1 Vrms
3	Audio Bandwidth 20Hz - 20 KHz	+/- 0.5 dB
4	SNR (A-weight)	>98 dB
5	THD + NOISE (A-weight, 0 dB input)	< -88 dB
6	Dynamic Range	94 dB
7	Channel Separation	< -96 dB
8	Nonlinear Distortion	< 0.25 dB
9	Channel Gain Error	< 0.5 dB

All Measurement were taken with only one channel active.

Description (continue)

The DAC support conversion rate from 32K to 192KHz while the ADC from 32K to 96K. The CE2836 support 32, 24, 20 and 16-bit input data. It also support multiple sampling frequency data. Each DAC has its own individual volume control.

XCK REQUIREMENT

The CE2836 supports 32K, 44.1K, 48K, 96K and 192K sampled audio in DAC operations and32K, 44.1K, 48K and 96K sampled audio in ADC operations. The oversampled clock, XCK, requirements are listed in Table 1 and 2.

The DAC and ADC PCM serial port can be configured as '*Master*' or *'Slave*' independently and each has separated over sampling clock input. In the '*Slave Mode*' PCM serial port operation if the AUTODEC, CR1[7]==1,there is an clock frequency detection circuit to set up the system clock, the users don't need to set the SRC registers. However in the '*master mode*' operation the users need to set the SCR registers for the serial audio clock generations

Table 1.

Sampling Rate	**DAC XCK Requirement**				
		DACDIV==0		DACDIV==1	
32 K	**XCK Freq**	12.288 MHz	8.192 Mhz.	24.576 Mhz	16.384 Mhz
	SRC[1:0]	[11], 384 fs	(#), 256 fs	[11], 768fs	(#), 512 fs
44.1K	**XCK Freq**	16.934 Mhz	11.29 Mhz.	33.869 Mhz	22.579 Mhz
	SRC[1:0]	[11], 384fs	[10], 256 fs	[11], 768 fs	[10], 512fs
48 K	**XCK Freq**	18.432 MHz	12.288 Mhz	36.864 MHz	24.576 Mhz.
	SRC[1:0]	[11], 384 fs	[10], 256 fs	[11], 768fs	[10], 512 fs
96 K	**XCK Freq**	18.432 MHz	12.288 Mhz.	36.864 MHz	24.576 Mhz.
	SRC[1:0]	[01], 192 fs	[00], 128 fs	[01], 384 fs	[00], 256 fs
192 K	**XCK Freq**	18.432 Mhz	12.288 Mhz.	36.864 MHz	24.576 Mhz.
	SRC	(#), 96 fs	(#), 64 fs	(#), 192 fs	(#), 128 fs

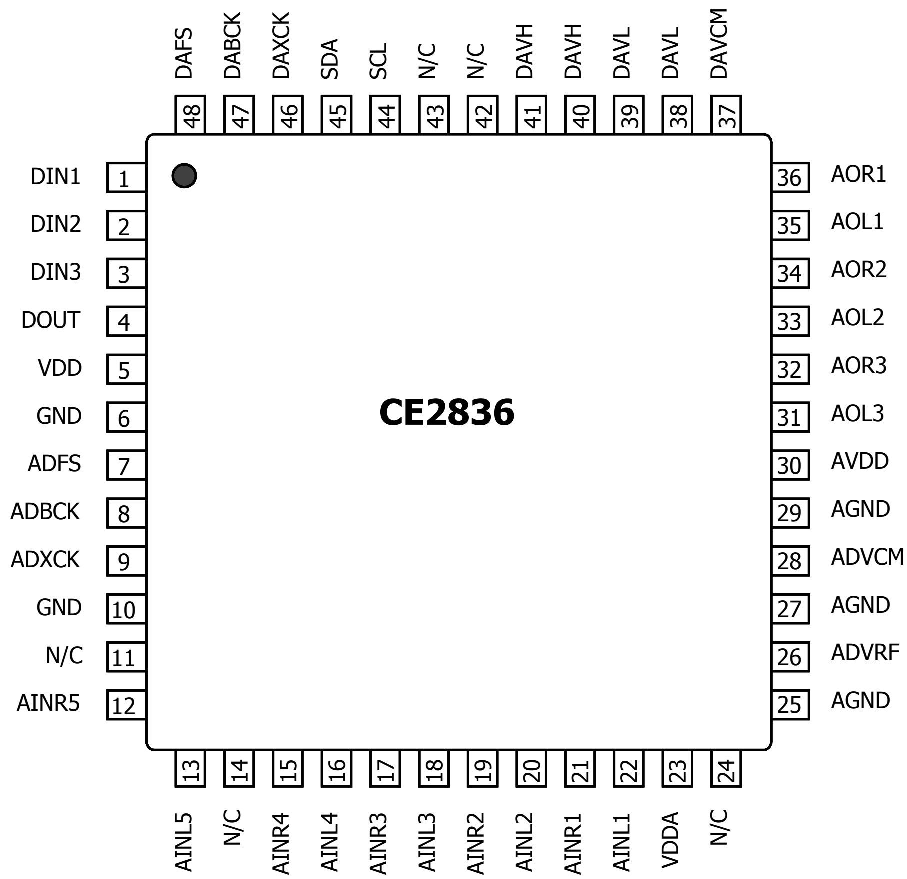
All the XCK clock rate listed are supported in the 'Slave Mode'
SRC Registers are used in the '*Master Mode*'. (#) are not supported in the in the 'Master Mode' .
DAC AUTODET is CREG1[7], DAC SRC[1:0]are CREG1[6:5] and DACDIV is CREG1[4].

Table 2.

Sampling Rate	**ADC XCK Requirement**				
		DACDIV==0		DACDIV==1	
32 K	**XCK Freq**	12.288 MHz	8.192 Mhz.	24.576 Mhz	16.384 Mhz
	SRC[1:0]	[10], 384 fs	(#), 256 fs	[10], 768fs	(#), 512 fs
44.1K	**XCK Freq**	16.934 Mhz	11.29 Mhz.	33.869 Mhz	22.579 Mhz
	SRC[1:0]	[10], 384fs	[00], 256 fs	[10], 768 fs	[00], 512fs
48 K	**XCK Freq**	18.432 MHz	12.288 Mhz	36.864 MHz	24.576 Mhz.
	SRC[1:0]	[10], 384 fs	[00], 256 fs	[10], 768fs	[00], 512 fs
96 K	**XCK Freq**	18.432 MHz	12.288 Mhz.	36.864 MHz	24.576 Mhz.
	SRC[1:0]	[11], 192 fs	[01], 128 fs	[11], 384 fs	[01], 256 fs

All the XCK clock rate listed are supported in the ‘Slave Mode’ .
SRC Registers are used in the ‘*Master Mode*’. (#) are not supported in the ‘Master Mode’ .
ADC AUTODETis CREG9[7], DAC SRC[1:0]are CREG9[6:5] and DACDIV is CREG9[4].

PIN ASSIGNMENT



PIN DESCRIPTION

Pin Name	Pin #	Type	Description
DIGITAL			
N/C	43		No connection. It can be tied to GND.
SDA	44	I/O	Serial command port data line.
SCL	45	I	Serial command port clock line.
DAXCK	46	I	External master clock input for DAC.
DABCK	47	I	DAC audio serial data clock Input pin (default) if DAC I/F is configured to be 'slave' else it is an Output.
DAFS	48	I	DAC left/right channel clock pin. Please refer to Figure 1 PCM data format for its definition Input (default) if DAC I/F is configured to be 'slave' else it is an output
DIN1	1	I	DAC Channel 1 or TDM serial audio data input.
DIN2	2	I	DAC Channel 2 serial audio data input.

PIN DESCRIPTION (Continued)

Pin Name	Pin #	Type	Description
DIN3	3	I	DAC Channel 3 serial audio data input.
DOUT	4	O	Serial ADC output
VDD	5	+3.3V	Digital power supply, 3.3 Volt.
GND	6	GND	Digital ground
ADFS	7	I/O	ADC left/right channel clock pin. Please refer to Figure 1 PCM data format for its definition. Input (default) if ADC I/F is configured to be *'slave'* else it is an output
ADBCK	8	I/O	External master clock input for ADC. Input (default) if ADC I/F is configured to be *'slave'* else it is an output
ADXCK	9	I	ADC audio serial data clock input.
GND	10	I	Digital ground
Analog			
N/C	11		No connection. It can be tied to AGND.
AINR5	12	I	ADC channel 5 right input. Input resistance is 20K Ohm
AINL5	13	I	ADC channel 5 left input. Input resistance is 20K Ohm
N/C	14		No connection. It can be tied to AGND.
AINR4	15	I	ADC channel 4 right input. Input resistance is 20K Ohm
AINL4	16	I	ADC channel 4 left input. Input resistance is 20K Ohm
AINR3	17	I	ADC channel 3 right input. Input resistance is 20K Ohm
AINL3	18	I	ADC channel 3 left input. Input resistance is 20K Ohm
AINR2	19	I	ADC channel 2 right input. Input resistance is 20K Ohm
AINL2	20	I	ADC channel 2 left input. Input resistance is 20K Ohm
AINR1	21	I	ADC channel 1 right input. Input resistance is 20K Ohm
AINL1	22	I	ADC channel 1 left input. Input resistance is 20K Ohm
AVDD	23	+3.3V	ADC power supply.
N/C	24		No connection. It can be tied to AGND.
AGND	25	GND	Analog ground pin.
ADVRF	26	O	ADC reference voltage. It should be decoupled to AGND with a 22 uF capacitor in parallel with a 0.1 uF. Its value should be AVDD/2 volt.
AGND	27	GND	Analog ground pin.

PIN DESCRIPTION (Continued)

Pin Name	Pin #	Type	Description
ADVCM	28	O	ADC comment mode voltage. It should be decoupled to AGND with a 22 uF in parallel with a 0.1 uF. Signal level is AVDD/2.
AGND	29	GND	Analog ground pin.
AVDD	30	+3.3V	DAC power supply.
AOL3	31	O	Analog left channel 3 output
AOR3	32	O	Analog right channel 3 output
AOL2	33	O	Analog left channel 2 output
AOR3	34	O	Analog right channel 2 output
AOL1	35	O	Analog left channel 1 output
AOR1	36	O	Analog right channel 1 output
DAVCM	37	O	DAC comment mode voltage. It should be connected to a 22 uF in parallel with a 0.1 uF decoupling capacitors to ground. Signal level is AVDD/2.
DAVL	38, 39	GND	DAC negative reference voltage. It should be tied to AGND.
DAVH	40,41	I	DAC positive reference voltage. It should be connected to AVDD via a 180 ohm serial resistor, and a 22 uF in parallel with a 0.1 uF decoupling capacitors to ground.
N/C	42		No connection. It can be tied to AGND.

DIGITAL AUDIO SERIAL INTERFACE

There are two independent PCM serial ports, one for DAC and one for ADC. The DAC digital serial interface consists of 3 serial input pins, DIN1, DIN2, DIN3, one serial clock input/output pin, DABCK, and one left/right indicator input/output pin, DAFS. The ADC consists of a data output pin, DOUT and one serial clock input/output pin, ADBCK, and one left/right indicator input/output pin, ADFS. The BCK and FS are output pins when the respective port is configured as *'Master*', and input pin when it is configured as '*Slave*' port. The Master/Slave operations are setup via CREGA[7] and CREGA[3]. The data are 2's complement MSB first numbers. The CE2836 supports four resolution, which are selected programming the control register CREG0 and CRFEGA via the I^2C serial control port. Table 3 describes these four resolution.

Table (3): Audio Serial Data Input Resolution,

Format	NBIT[1:0]	DIN, DOUT
0	00	16-bit
1	01	20-bit
2	10	24-bit (default)
3	11	32-bit

The DIN and DOUT can be either 24-bit or 32-bit per frame as well as left justified, right justified or I2S. .

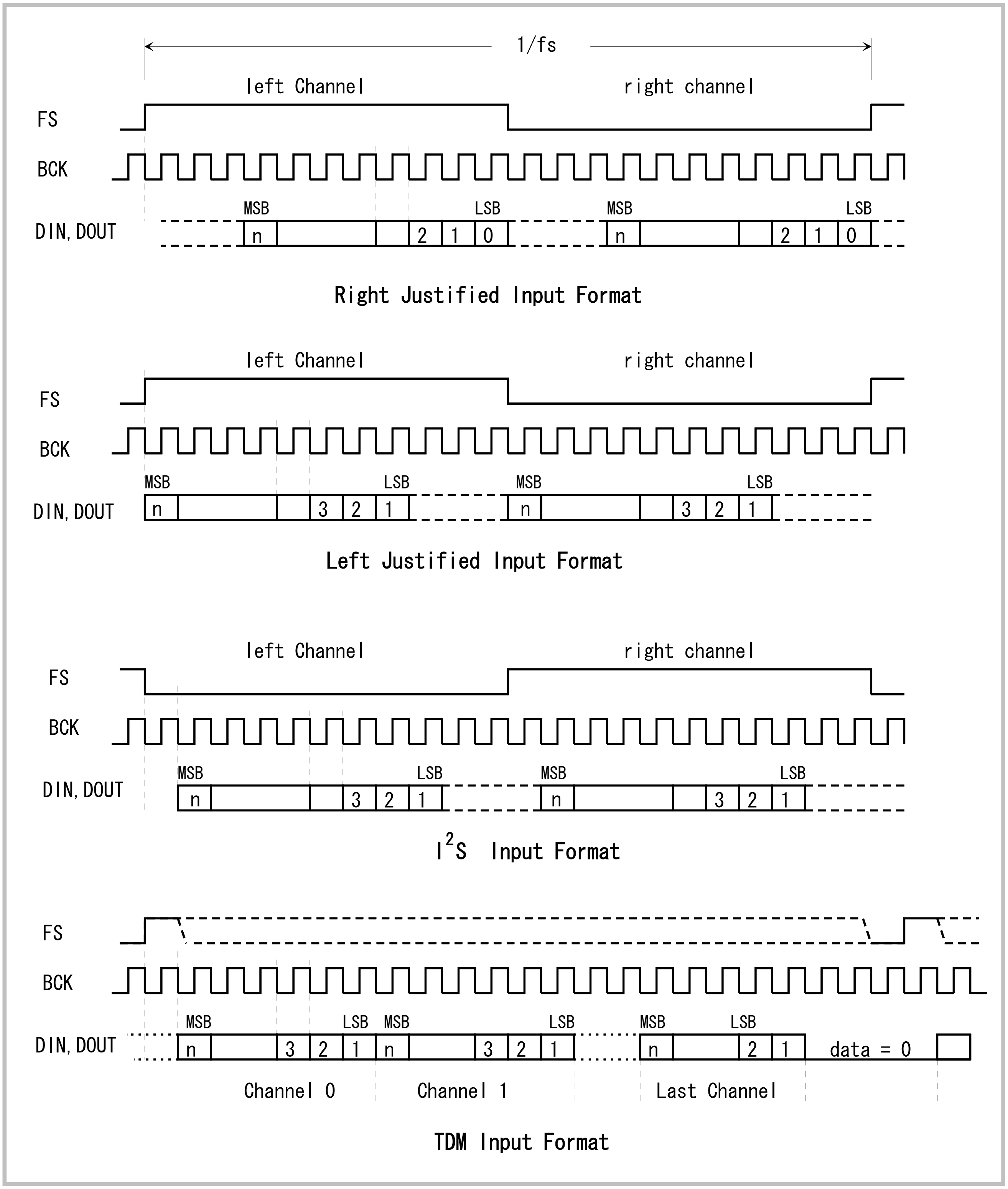
Table (4): Audio Serial Data Input Modes

Mode	FMT[1:0]	DIN, DOUT
0	00	Right Justified
1	01	Left Justified
2	10	I2S (default)
3	11	TDM

TDM Input Format

The CE2836 support Time Division Multiplex data input. In this format only one data input pin is required. The six channel data are sent in serial order, channel 1 first, followed by channel 2 and so forth. The number of bits per channel is defined by CREG0[5:4].

Figure 1. Audio Serial Input Data Format



DAC INFINITE ZERO DETECTION

The CE2836 DAC has an Infinite Zero Detection circuit which detects zero in the Audio Serial Port that lasts for approximately 0.2 sec. By default, the zero detection circuit is on.

DAC Digital Attenuation

Each DAC contains an Digital Attenuation block. The attenuation values are hold in the Volume Control Registers. The Value 80H corresponds to Full Scale, 0dB. and each decrement correspond to -0.5 dB additional attenuation.

ADC Gain and ALC

Each channel of ADC input includes a Analog Gain. The Gain is controlled by CREGC, ADC Gain Selection, The gain range is from +6 dB to -9 dB. with 1 dB step. The GAIN = 9 corresponds to 0dB gain. The AUTOMATIC LEVEL CONTROL set the ADC maximum digital output to a prescribed value by automatic manipulating the analog gain. The ALC is controlled by CREG8, ADC PROC. REGISTER..

Table (5): ALC Target Level

ALC[2:0]	Maximum Digital Output
000	-1 dB FS
001	-2 dB FS
010	-3 dB FS
011	-4 dB FS
100	-5 dB FS
101	-6 dB FS
110	-7 dB FS
111	-8 dB FS

Table (6): ALC Hold Time

ALCHTM	Hold Time	Comment
0	340 msec.	For music program
1	5.3 msec	For speech program

ADC Noise Gate

Noise Gate remove hissing noise during silence period. It is useful for recording noisy program. While Noise Gate is enabled the ADC digital output will be zeroed if the signal level below a predetermined value for about 0.5 seconds. The noise Gate is controlled by the same ADC PROC. REGISTER.

Table (7): Noise Gate Threshold

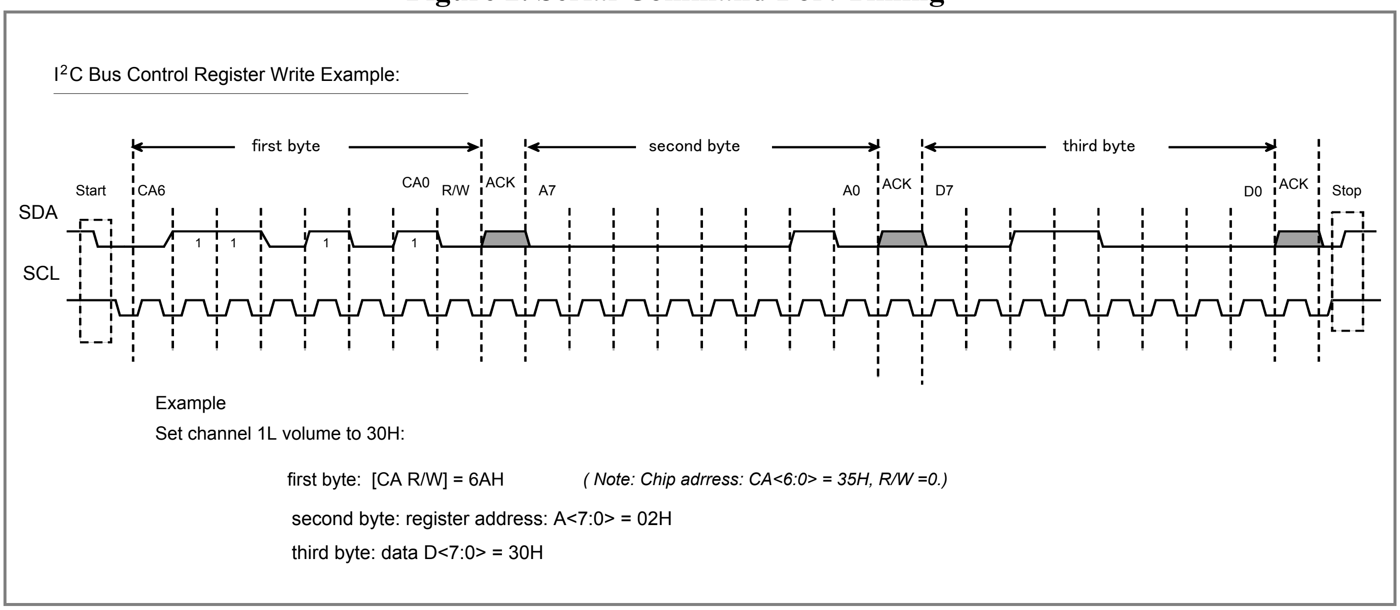
NGTH[1:0]	Threshold
00	-66 dB
01	-72 dB
10	-78 dB
11	-84 dB

Serial Command Port

The user can select the chip operation mode by programming the internal control registers through serial I^2C port. The Chip Address for the CE2836 is 35H. The protocol for write operation consists of sending 3 byte data to CE2836, following each byte is the acknowledges generated by CE2836. The first byte is the 7-bit Chip Address followed by the read/write bit (read is high, write is low). The second byte is the control register address. The third byte is the control register data.

Upon power up, all programmable registers are set to default values. Figure 2 describes the serial command port timing relationship.

Figure 2. Serial Command Port Timing



SERIAL PORT CONTROL REGISTER ASSIGNMENT

There are 8 registers dedicated to the CE2836 for chip functional programming, The register addresses assignments are

Address (decimal)	Register	Default Value	Register Function
0	CREG0[7:0]	A0	DAC Control REG0: Data input format, de-emphasis filter selection
1	CREG1[7:0]	80	DAC Control REG1: Input format and PLL output frequency selection
2	CREG2[7:0]	80	Volume Control Register for DAC channel 1, left
3	CREG3[7:0]	80	Volume Control Register for DAC channel 1, right
4	CREG4[7:0]	80	Volume Control Registerl for DAC channel 2, left
5	CREG5[7:0]	80	Volume Control Register for DAC channel 2, right
6	CREG6[7:0]	80	Volume Control Register for DAC channel 3, left
7	CREG7[7:0]	80	Volume Control Registerl for DAC channel 3, right
8	CREG8[7:0]	82	ADC Proc REG: ALC and Noise Gate Control Registers
9	CREG9[7:0]	A0	ADC Control Register.
10	CREGA[7:0]	00	CHIP Control Register.
11	CREGB[7:0]	01	ADC MUX Select.
12	CREGC[7:0]	99	ADC Input Gain Select
13	CREGD[7:0]	92	Chip Soft Reset.

CONTROL REGISTERS DESCRIPTION

CREG0, DAC Control Register 0 (ADRS=hex00, default=hexA0)

ADDR[3:0]	CREG0[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 00	FMT[1:0]		NBIT[1:0]		AMUTE	DEEMP	FSMPL[1:0]	
Default Value	1	0	1	0	0	0	0	0

FMT[1:0] Digital Serial Bus Format Select
- 00: - Normal or Right Justified Format.
- 01: -Left Justified Format.
- 10: - I2S Format.(default)
- 11: - TDM, Multi-channel Time Division Multiplex Format

NBIT[1:0]: - These two bits define the serial audio input resolution for right justified and TDM mode
- 00: - 16-bit resolution.
- 01: - 20-bit resolution.
- 10: - 24-bit resolution (default).
- 11: - 32-bit resolution.

AMUTE: - Auto-mute detection enable.
- 0: - Auto-mute enabled. (default)
- 1: - No auto-mute.

DEEMP: - Enable de-emphasis
- 0: - Normal. (default)
- 1: - enable de-emphasis.

FSMPL: - Interpolation filter selection.

These two bits are recognized only when "AUTODET" bit of the CREG1 is set to '0'.
- 0X: - 44.1 or 48K sampling.(default)
- 10: - 96K sampling.
- 11: - 192K sampling.

CREG1, DAC Control Register 1(ADRS=hex01, default=hex80)

ADDR[3:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 01	AUTODET	SRC[1:0]		CKDIV2	X	MUTE56	MUTE34	MUTE12
Default Value	1	0	0	0	0	0	0	0

AUTODET Automatically detects the serial audio input data sampling rate clock frequency.
0: - do not use auto-detect
1: - automatically detects the serial audio input data sampling rate and clock frequency.

SRC[1:0]: - DAC Sampling Rate Selection. It is used in the DAC Master Mode, CRA[7]==1, to generate DAFS and DABCK.

00: - Sampling Rate = XCK/128.
01: - Sampling Rate = XCK/192.
10: - Sampling Rate = XCK/256.
11: - Sampling Rate = XCK/384.

CKDIV2: - Enable the ADXCK Clock divided by 2.
0: - DAC system clock is DAXCK (default)
1: - DAC system clock is DAXCK/2

MUTE56: Mute control for channels 5 and 6
0: do not mute channels 5 and 6
1: simultaneously mute channels 5 and 6

MUTE34: Mute control for channels 3 and 4
0: do not mute channels 3 and 4
1: simultaneously mute channels 3 and 4

MUTE12: Mute control for channels 1 and 2
0: do not mute channels 1 and 2
1: simultaneously mute channels1 and2

CREG2 - 7, DAC Volume Registers for channel 1 to 6, (ADRS=hex02 - hex07, default=hex80)

ADDR[3:0]	Volume Registers							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 02	Channel 1 left volume register, VOLREGL1[7:0]							
Hex 03	Channel 1 right volume register, VOLREGR1[7:0]							
Hex 04	Channel 2 left volume register, VOLREGL2[7:0]							
Hex 05	Channel 2 right volume register, VOLREGR2[7:0]							
Hex 06	Channel 3 left volume register, VOLREGL3[7:0]							
Hex 07	Channel 3 right volume register, VOLREGR3[7:0]							
Default Value	1	0	0	0	0	0	0	0

VOLREG:- Control the volume of the 6 DAC's

80h corresponds to 0 dB and 02h to -64 dB. in -0.5 db step. Value should not be programmed greater than 80h.

CREG 8, ADC Proc Register (ADRS=hex08, default=hex82)

ADDR[3:0]	CREG0[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 08	NGATE	NGTH[1:0]		ALCHTM	ALCEN	ALC[2:0]		
Default Value	1	0	0	0	0	0	1	0

NGATE: Noise Gate
- 0: - Noise Gate Disabled.
- 1: -Noise Gate Enable. When the signal level is lower than the level specified by the NGTH the ADC output will be zeroed.

NGTH[1:0]: - Specified the Noise Gate Threshold.
- 00: - -66dB
- 01: - -72 dB.
- 10: - -78dB.
- 11: - -84 dB.

ALCHTM: - Automatic Level Control Hold time.
- 0: - 340 ms. (default). For music program.
- 1: - 5.3 ms. This should be used for speech conversion.

ALCEN: - Enable Automatic Level Control Function
- 0: - Disable ALC. (default)
- 1: - Enable ALC.

ALC[2:0]: - ALC Target Level.
- 000: - -1 dB.
- 001: - -2 dB.
- 010: - -3 dB. (default)
- 011: - -4 dB.
- 100: - -5 dB.
- 101: - -6 dB.
- 110: - -7 dB.
- 111: - -8 dB.

CREG9, ADC Control Register (ADRS=hex09, default=hexA0)

ADDR[3:0]	CREG0[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 09	FMT[1:0]		NBIT[1:0]		X	SRC[1:0]		CKDIV2
Default Value	1	0	1	0	0	0	0	0

MT[1:0] Digital Serial Bus Format Select for ADC.
- 00: - Normal or Right Justified Format.
- 01: -Left Justified Format.
- 10: - I2S Format.(default)
- 11: - TDM, Multi-channel Time Division Multiplex Format

NBIT[1:0]: - These two bits define the ADC serial audio input resolution for right justified and TDM mode
- 00: - 16-bit resolution.
- 01: - 20-bit resolution.
- 10: - 24-bit resolution (default).
- 11: - 32-bit resolution.

SRC[1:0]: - ADC Sampling Rate Selection. It is used in the ADC Master Mode, CRA[1]==1, to generate ADFS and ADBCK.

- 00: - Sampling Rate = XCK/256.
- 01: - Sampling Rate = XCK/128.
- 10: - Sampling Rate = XCK/384.
- 11: - Sampling Rate = XCK/192.

CKDIV2: - Enable the ADXCK Clock divided by 2.
- 0: - ADC system clock is ADXCK (default)
- 1: - ADC system clock is ADXCK/2

CREGA, Chip Control Register (ADRS=hex0A, default=hex00)

ADDR[3:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 0A	DAMSTR	DAPWD	X	X	ADMSTR	ADPWD	ZCBYP	HPFBYP
Default Value	0	0	0	0	0	0	0	0

DAMSTR: Configure the DAC PCM Serial Port.
- 0: - Slave Mode
- 1: - Master Mode.

DAPWD: DAC Power Down
- 0: DAC enabled
- 1: DAC Power Down.

ADMSTR: Configure the ADC PCM Serial Port.
- 0: - Slave Mode
- 1: - Master Mode.

ADPWD: ADC Power Down
- 0: ADC enabled
- 1: ADC Power Down.

ZCBYP: Disable ADC Zero Crossing Detection
- 0: Zero crossing is enabled.
- 1: Zero crossing is bypassed.

HPFBYP: Bypass ADC data path High Pass Filter
- 0: Enable high pass filter.
- 1: Disable high pass filter.

CREGB, ADC Input Enable (ADRS=hex0B, default=hex01)

ADDR[3:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 0B	X	X	X	AMUX[4:0]				
Default Value	1	0	0	0	0	0	0	1

AMUX[4:0]: ADC Input Channel Enable.

00001: - AIN1
00010: - AIN2
00100: - AIN3
01000: - AIN4
10000: - AIN5

CREGC, ADC Input Gain Selection (ADRS=hex0C, default=hex99)

ADDR[3:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 0C	LGAIN[3:0]				RGAIN[3:0]			
Default Value	1	0	0	1	1	0	0	1

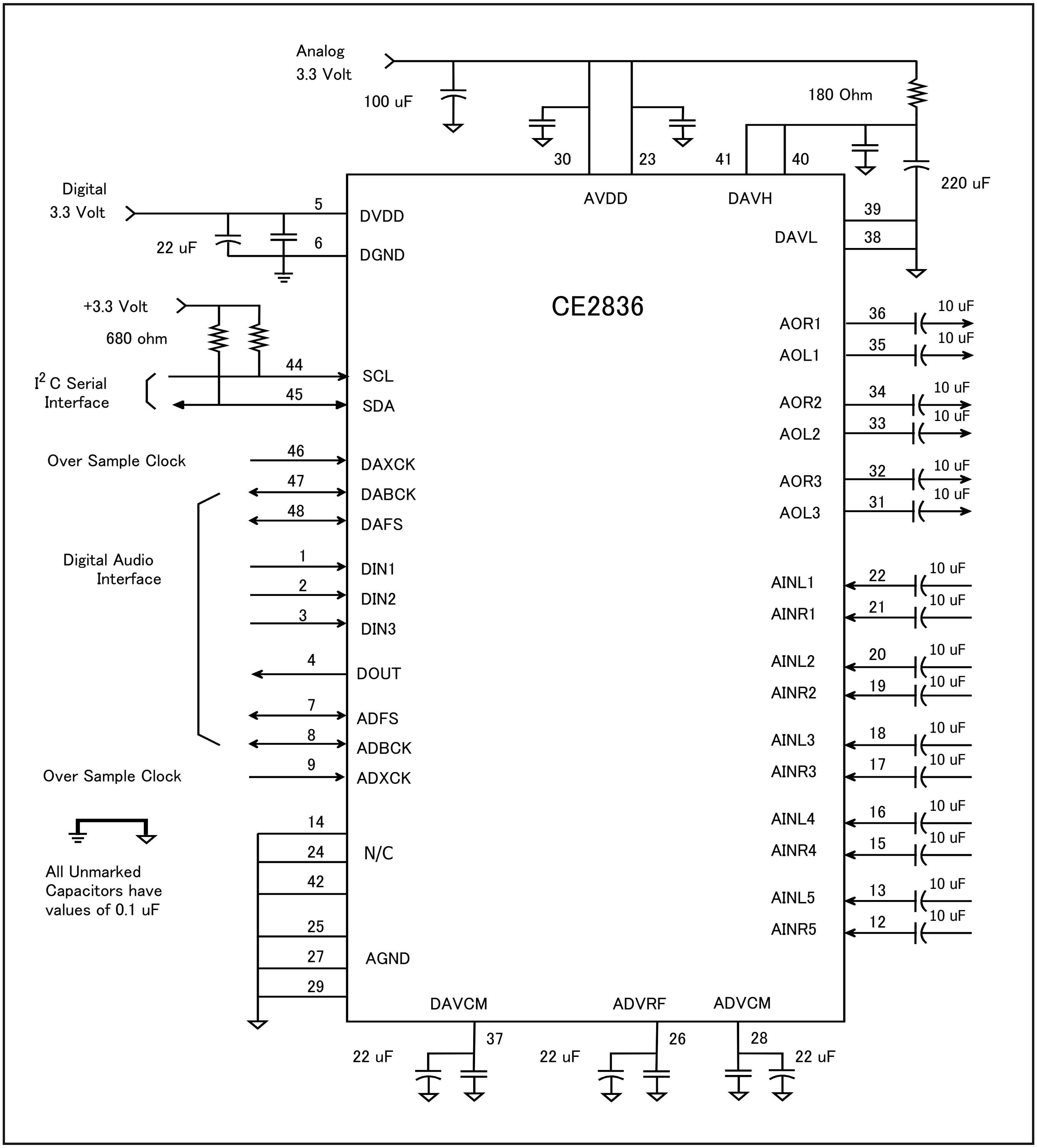
LGAIN[3:0] is for ADC Left Channel Gain Select While RGAIN[3:0] is for Right Channel Gain Select
1111 corresponds to +6 dB and 0000 to -9 dB with -1dB step

CREGD, Chip Soft Reset (ADRS=hex0D, default=hex92)

ADDR[3:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 0D	RESET[7:0]							
Default Value	1	0	0	1	0	0	1	0

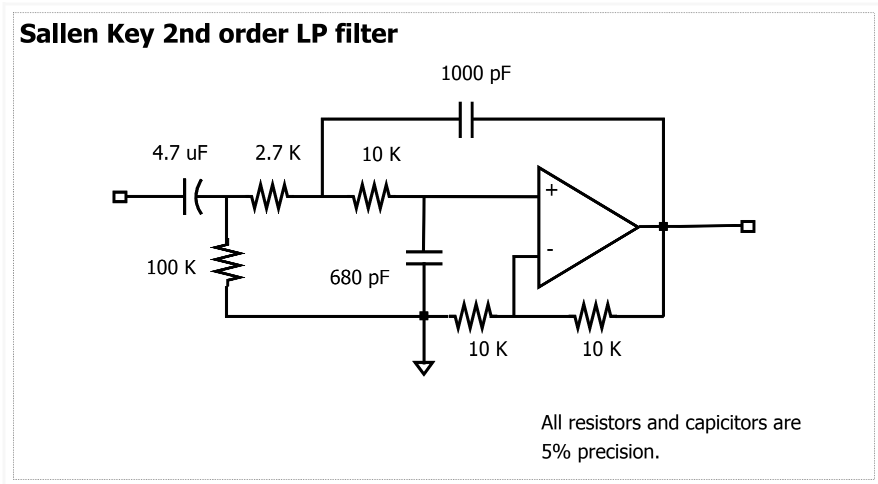
Chip Soft Reset; A write of all zeros to this register will reset the chip except the Command Registers. Another write of hex92 is required to enable to chip again.

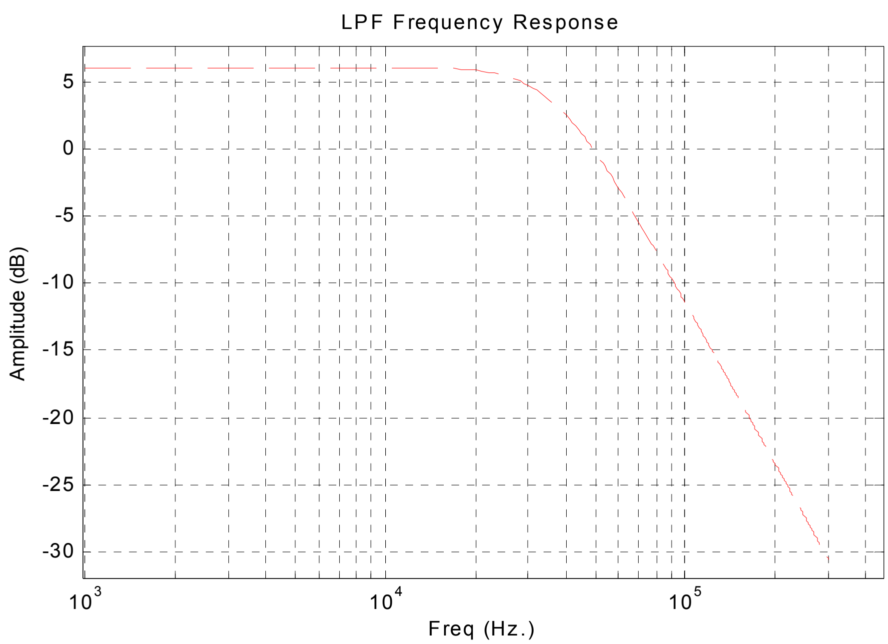
APPLICATION CONNECTION EXAMPLE:



SUGGESTED ANALOG RECONSTRUCTION FILTER

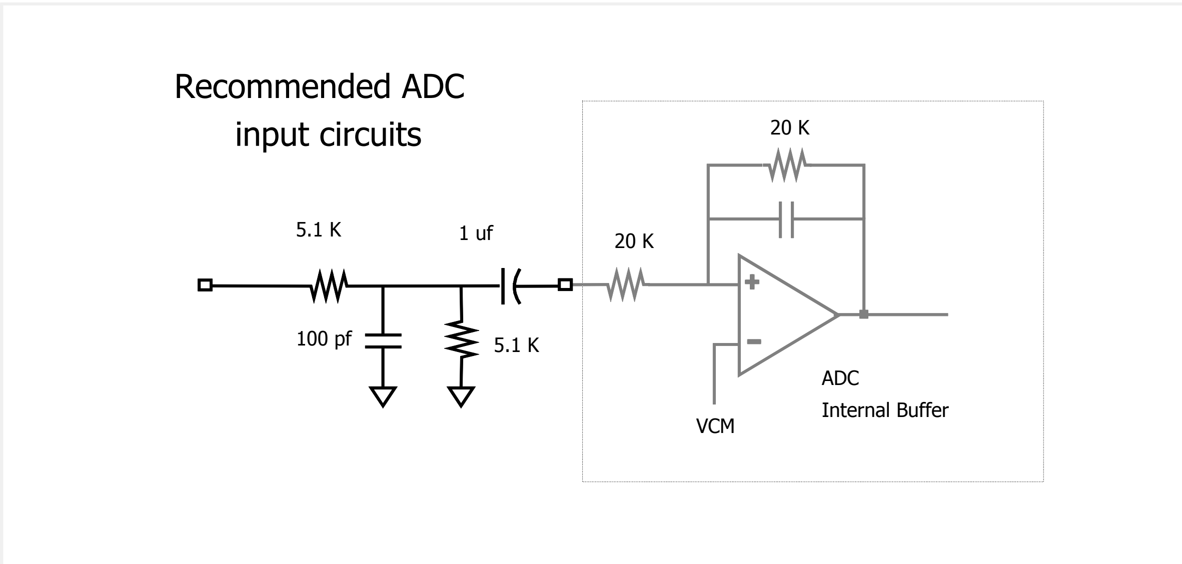
A second Sallen Key low pass reconstruction filter is recommend to remove the high frequency sigma delta modulator noise. The filter's component values and characteristic are shown in the following figures.





ADC

The ADC converters have a input buffer. The buffers have a equivalent input resistance of 20K ohm. To ensure the performance it is recommended that the applications should have a simple low pass filter to remove the high frequency noise.



TIMING DIAGRAM

Figure 3. Audio Serial Interface Timing Requirement

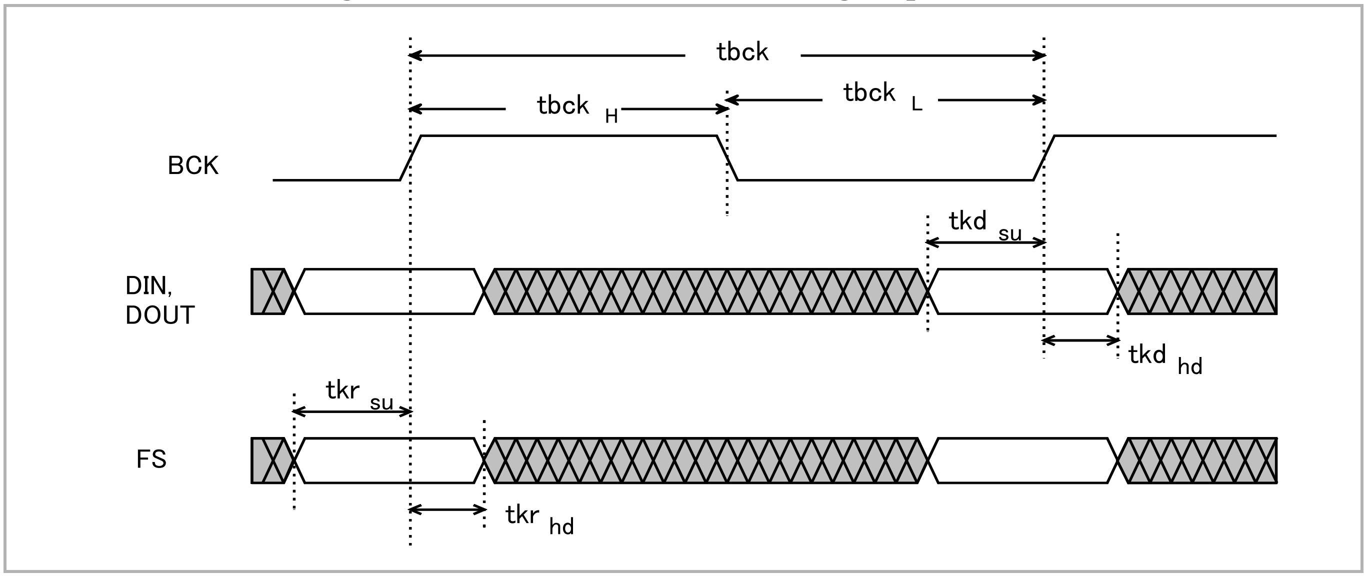
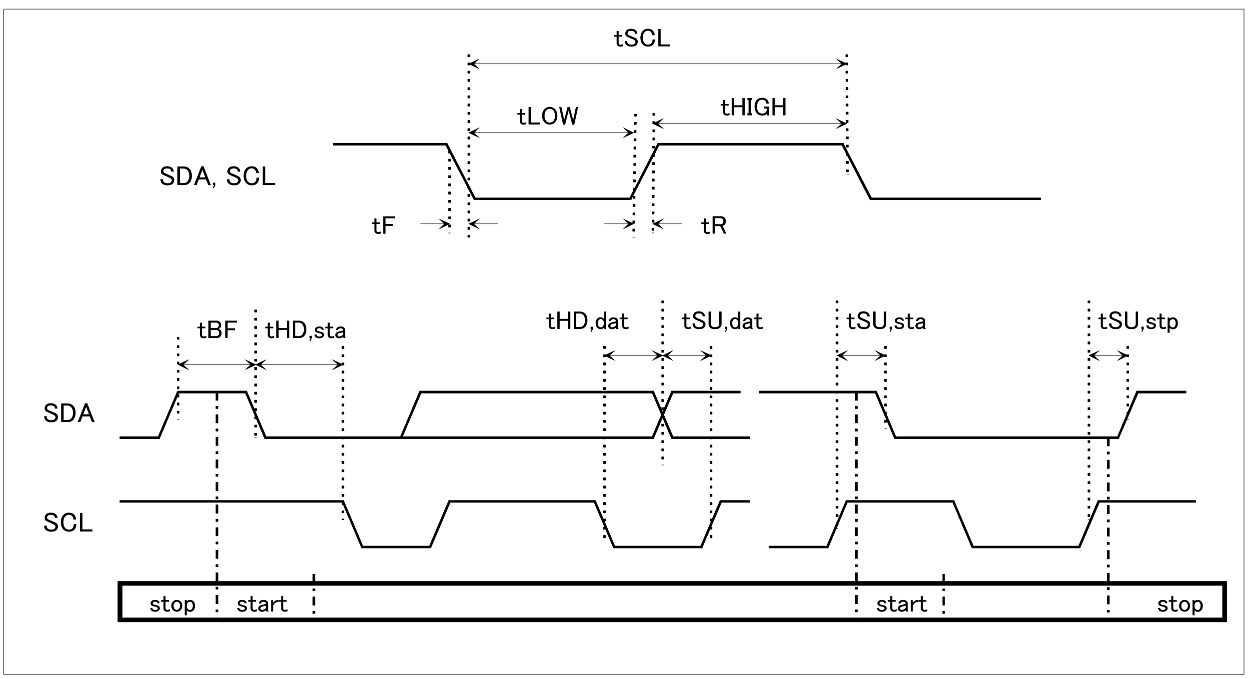


Figure 4. Serial Command Port Write Timing Requirement



ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristics	Min	Max	Units
V_{DD}	Power Supply Voltage (Measured to GND)	-0.5	+7.0	V
V_i	Digital Input Applied Voltage[2]	GND-0.5		V
A_i	Digital Input Forced Current[3,4]	-100	100	mA
V_o	Digital Output Applied Voltage[2]	GND-0.5	V_{DD}+0.5	V
A_o	Digital Output Forced Current[3,4]	-100	100	mA
TDsc	Digital Short Circuit Duration (single output high state to Vss)		1	Sec
TA_{SC}	Analog Short Circuit Duration (single output to VSS1)		infinite	Sec
T_a	Ambient Operating Temperature Range	-25	+125	^oC
T_j	Junction Temperature (Plastic Package)	-65	+150	^oC
Tsol	Lead Soldering Temperature (10 sec., 1/4” from pin)		280	^oC
Tvsol	Vapor Phase Soldering (1 minute)		220	^oC
Tstor	Storage Temperature	-65	+150	^oC

Notes:

1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.

2. Applied voltage must be current limited to specified range, and measured with respect to VSS.

3. Forcing voltage must be limited to specified range.

4. Current is specified as conventional current, flowing into the device.

ELECTRICAL CHARACTERISTICS

Parameter	Characteristics	Min	Typ	Max	Units
Power Supply					
AVDD	Analog power supply voltage	2.8	3.3	4.0	V
DVDD	Digital power supply voltage	2.8	3.3	4.0	V
I_{DA}	Analog Current		60		mA
I_{DD}	Digital Current		20	18	mA

Audio DAC Characteristics

	Full Scale Output Voltage to a 10K load	.98	1	1.02	Vrms
$V_{\mathbf{VCM}}$	Reference voltage		VDD/2		V

Digital Characteristics

V_{IH}	Digital Input Voltage, Logic HIGH, TTL Compatible Inputs.	2.0		V_{DD}	V
I_{OZH}	Hi-Z Leakage Current, HIGH, V_{DD}=Max, V_{IN}=3.3 Volt			33	μ A
I_{OZL}	Hi-Z Leakage Current, LOW, V_{DD}=Max, V_{IN}=$V_{SS)}$			-10	μ A
C_I	Digital Input Capacitance (T^A=25°C, f=1Mhz)			8	pF
C_O	Digital Output Capacitance (T^A=25°C, f=1Mhz)			10	pF

Audio Serial Interface Timing

tbck	BCK Cycle Time	80			ns
$tbck_H$	BCK Pulse Width, HIGH	30			ns
$tbck_L$	BCK Pulse Width, LOW	30			ns
tkd_{su}	Audio Data Setup Time With Respect To Rising Edge of BCK	10			ns
tkd_{hd}	Audio Data Hold Time With Respect to Rising Edge of BCK	15			ns
tkr_{su}	Audio FS Setup Time With Respect To Rising Edge of BCK	10			ns

Parameter	Characteristics	Min	Typ	Max	Units
tkr_{hd}	Audio FS Hold Time With Respect To Rising Edge of BCK	15			ns

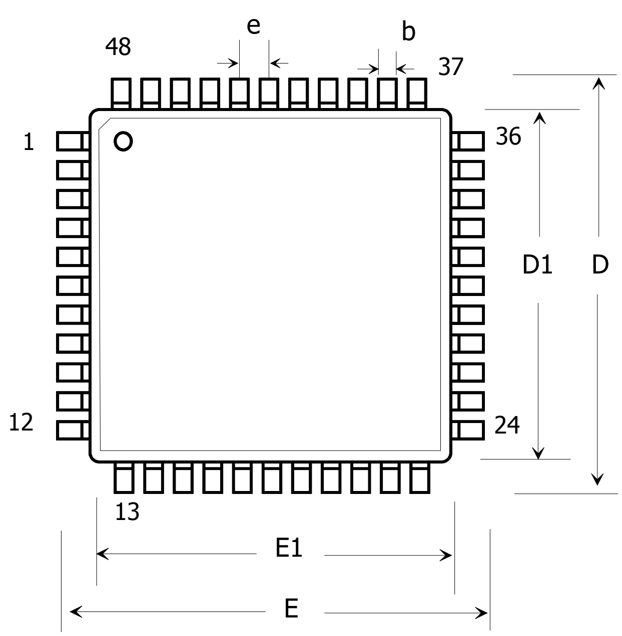
Serial Command Port

fSCL	SCL Clock Frequency			100	kHz
tSU,sta	Start condition set up time	4.7			us
tHD,sta	Start condition hold time	4.0			us
tSU,stp	Stop condition set up time	4.0			us
tLOW	SCL Low time	4.7			us
tHIGH	SCL High time	4.0			us
tR	SCL & SDA rise time			1.0	us
tF	SCL & SDA fall time			0.3	us
tSU,DAT	Data set-up time	250			ns
tHD,DAT	Data hold time	0			ns
tBF	Bus Free time	4.7			us

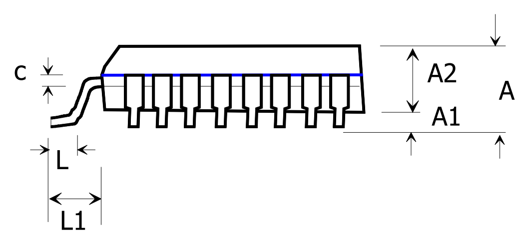
PACKAGING INFORMATION (LQFP 48 PIN)

Dimensions

SYMBOLS	mm.			SYMBOLS	mm.		
	min	norm	max		min	norm	max
A			1.68	E	9.0 BSC		
A1	0.05		0.15	E1	7.0 BSC		
A2	1.35	1.4	1.45	e	0.45	0.65	0.75
b	0.17	0.22	0.27	L	0.63	0.6	1.03
C	0.09		0.20	L1	1.00 REF		
D	9.0 BSC						
D1	7.0 BSC						



LQFP 48 (7 X 7 mm)



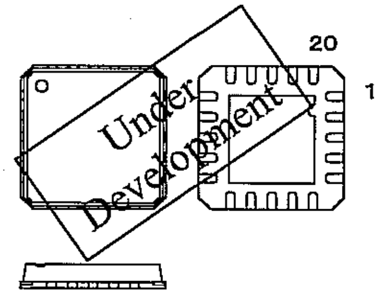
Digital Power Amplifier R2S15102NP

10Wx2ch(SE)/20Wx1ch(BTL) Digital Audio Power Amplifier

1.Outline

R2S15102NP is a Digital Power Amplifier IC developed for TV.
R2S15102NP can realize maximum Power 10W × 2ch
(VD = 24V,THD = 10%, SE) at 8 Ω load.
It is possible to replace from the conventional analog amplifier system to the digital amplifier system easily.

Fig. 1 Package



20pin QFN
Body : 6 x 6 mm
Lead pitch : 0.8 mm

2.Feature

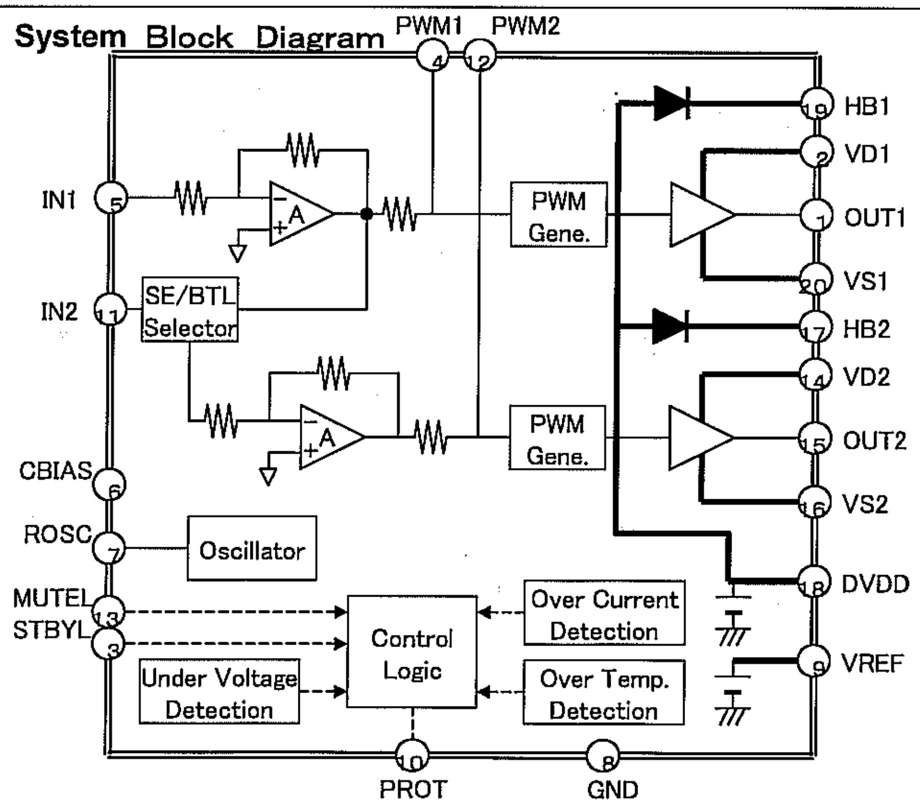
- High Output Power(THD=10%)without external Heat Sink
  (note) the thermal pad is soldered the thermal pad with the printed-circuit board directly.
  Recommanded Power Condition
  SE operation mode :10Wx2ch(VD=24V) at 8 Ω
  BTL operation mode: 20Wx1ch(VD=18V) at 8 Ω
- The RENESAS original circuits realize high power efficiency, low noise and low distortion characteristics.
- Pop sound Less
- Built-in protection function
  (Over Current, Over Temperature and Under Voltage)
- Built-in Mute and Stand-by function

3.Operating Condition

- Recommanded Power supply voltage : from 11V to 25V
- Recommanded Speaker Impedance : from 4 to 8Ω

4.Block Diagram

Fig. 2 System Block Diagram



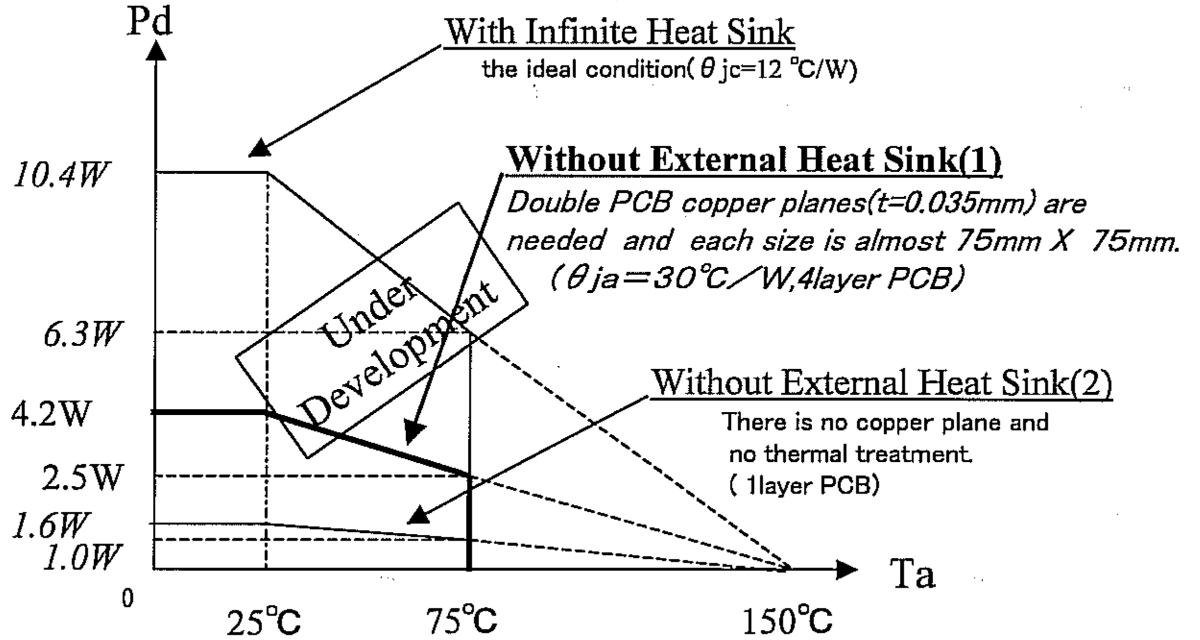
5. Pin Configuration(Table.1)

No.	NAME	I/O	Description
1	OUT1	O	Power Output pin #1
2	VD1	—	Power supply pin for power output stage #2
3	STBYL	I	Stand-by control pin. When this is "L", circuit current is reduced.There is the pull-down resistor:50Kohm(typ.).
4	PWM1	I	PWM input pin #1 (for phase compensation)
5	IN1	I	Analog input #1. The gain is depended on the external resistance .
6	CBIAS	I/O	A capacitor is connected so that it may not be influenced of power supply change(Ripple Filter).
7	ROSC	I	Control pin for PWM carrier frequency
8	GND	—	GND pin for analog block
9	VREF	I/O	Capacitor connection pin for analog block reference voltage source
10	PROT	O	Protection Timer pin. At protection mode,the output becomes "L"-level. (The timing capacitor is connected)
11	IN2	I	SE operation: Analog input #2(as same as IN1)
		I	BTL operation: When this is connected to DVDD pin via the resister, Reversed signal of OUT1 is output to OUT2.
12	PWM2	I	PWM input pin#2 (for phase compensation)
13	MUTEL	I	Mute control pin. When this is "L", it becomes mute status.
14	VD2	—	Power supply pin for power output stage #2
15	OUT2	O	Power Output pin #2
16	VS2	—	Ground pin for power output stage #2
17	HB2	I/O	Capacitor connection pin for bootstrap
18	DVDD	O	Built-in power supply pin for internal digital block.
19	HB1	I/O	Capacitor connection pin for bootstrap #1
20	VS1	—	Ground pin for power output stage #1

6. Absolute Maximum Rating(Table.2)

Symbol	Parameter	Condition	Value	Unit
VD max	Maximum VD Voltage	VD1,VD2 pin voltage	27	V
HB max	Maximum HB Voltage	HB1、HB2 pin voltage	40	V
Pd	Power dispassion	Ta = 25°C :See Fig.3	4.2	W
θja	Thermal Resistance	See Fig.3	30	°C/W
Tj	Junction temperature	Maximum Temperature	150	°C
Ta	Operating ambient temperature	Temperature range	-20～75	°C
Tstg	Storage temperature	Temperature range	-40～150	°C

Fig.3 Thermal De-rating(on PCB: printed-circuit board):Size 75mm x 75mm

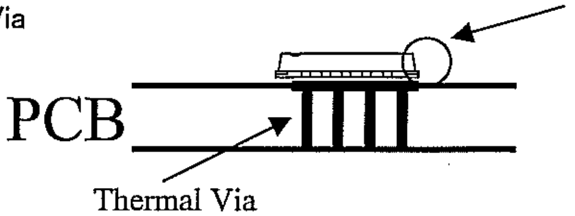


(NOTE)

PCB pattern design for high effective thermal conductivity

(1)The exposed die pad is directly soldered with the printed-circuit board pattern .

(2)Thermal Via



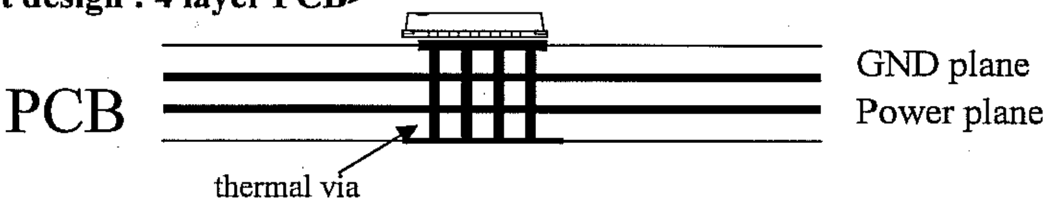
(caution)
There are side expositions of the die pad at corners of the package.
(The die pad is grounded.)

Consideration about the PCB design

The Power dispassion at 10Wx2ch(SE) or 20Wx1ch(BTL) is estimated almost 2W. It has enough margin, designing the PCB at θja=30°C/W.

(1)PCB basic design (copper plane)

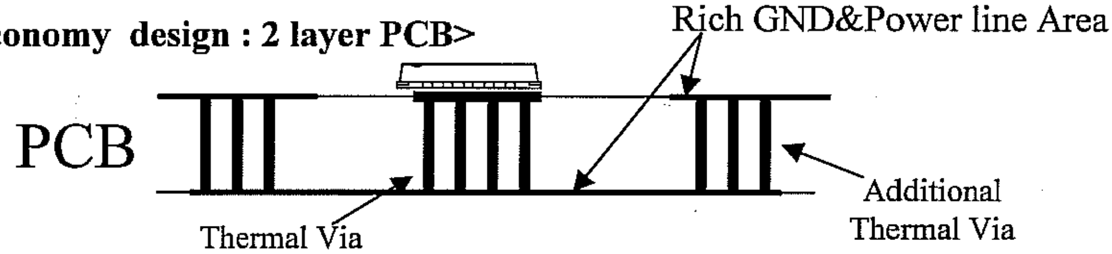
<the best design : 4 layer PCB>



<PCB size estimation >

10Wx2ch: 75mm x 75mm

<the economy design : 2 layer PCB>



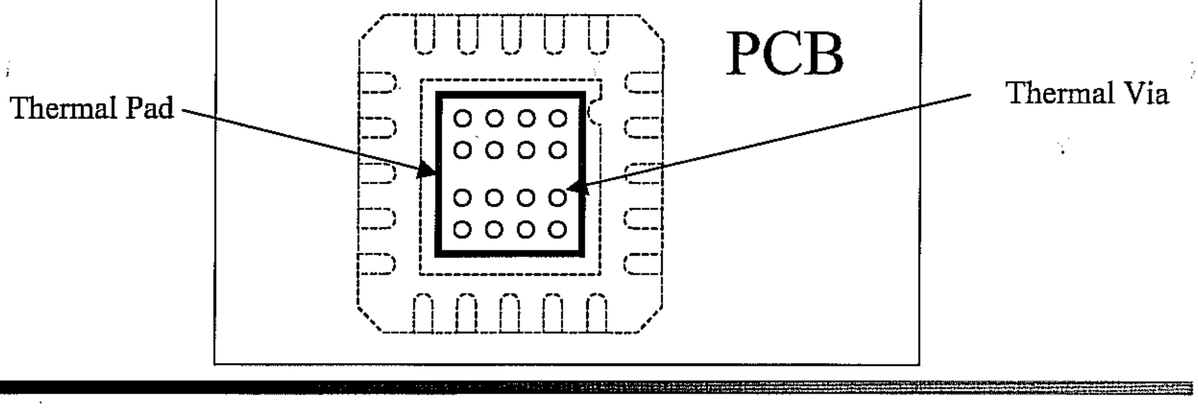
The GND&Power line total area size is also equal to the above GND&Power line total area size of the 4layer PCB.

<PCB size estimation >

10Wx2ch: (75+α)mm x (75+α) mm

(2)PCB Thermal Pad

The exposed die pad is directly soldered with the printed-circuit board pattern .



7. Recommended Operating condition(Table.3)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VD	Supply Voltage	VD1,VD2 pin voltage	11	-	25	V
VH	Control voltage of high level	STBYL、MUTEL	2	-	5	V
VL	Control voltage of low level	STBYL、MUTEL	0	-	0.8	V
fosc	Carrier Frequency	R= 33kΩ	300	400	600	kHz

(note)
- STBYL: High level:normal operation Low level:Stand-by
- MUTEL:High level:normal operation Low level:Mute
- The carrier frequency can be changed by the resistance at Pin#.7 .

8. Electronic Characteristics(Table.4)

(Unless otherwise noted, Ta=25°C, VD=24V, Carrier Frequency=400kHz, f=1kHz,SE operation)

Symbol	Parameter		Condition	MIN	TYP	MAX	Unit
IVD	Circuit Current		No Signal	TBD	28	TBD	mA
			MUTE	TBD	-	TBD	mA
			Stand-by	-	-	10	uA
VDPR	Detection Voltage		VD under-voltage	TBD	9.8	TBD	V
TPR	Protection Temperature		Thermal Shut-dawn	-	150	-	℃
TRL	Release Temperature		Thermal Shut-dawn	-	120	-	℃
IPR	Protection Current		Output over-current	-	6	-	A
Pomax	Maximum output power	at SE	THD=10%、VD=24V、RL=8Ω	TBD	10	-	W/ch
		at BTL	THD=10%、VD=18V、RL=8Ω	TBD	20	-	W
THD	Total Harmonic Distortion		Po=1W	-	0.1	TBD	%
No	Output Noise level		A-Weighted filter	-	(100)	TBD	uVrms
Eff	Power Efficiency	at SE	Po=10+10W	TBD	93	-	%
		at BTL	Po=20W	TBD	89	-	%
Mute	Mute Attenuation			TBD	80	-	dB
PSRR	Ripple Rejection Ratio		dVD=100mVrms,f=100 Hz	TBD	50	-	dB

9. Application Examples

(note)
"R for GND" 's are for the evaluation only and not needed actually.

Fig.4 SE operation mode(10Wx2ch)

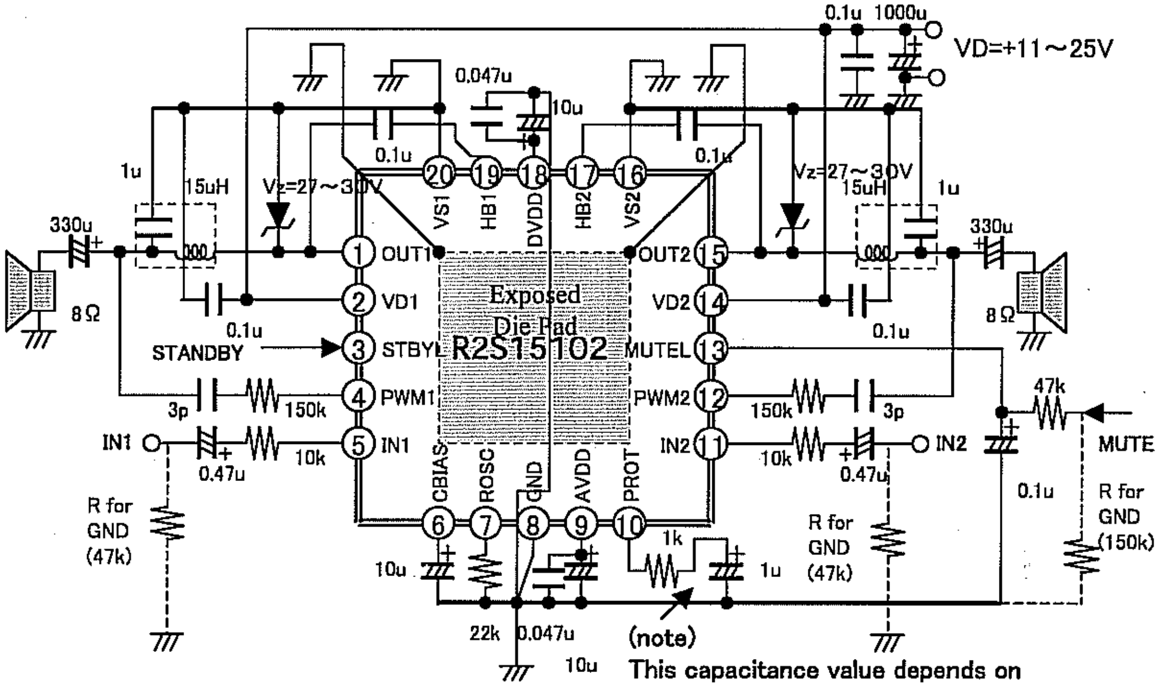


Fig.5 BTL operation mode (20W)

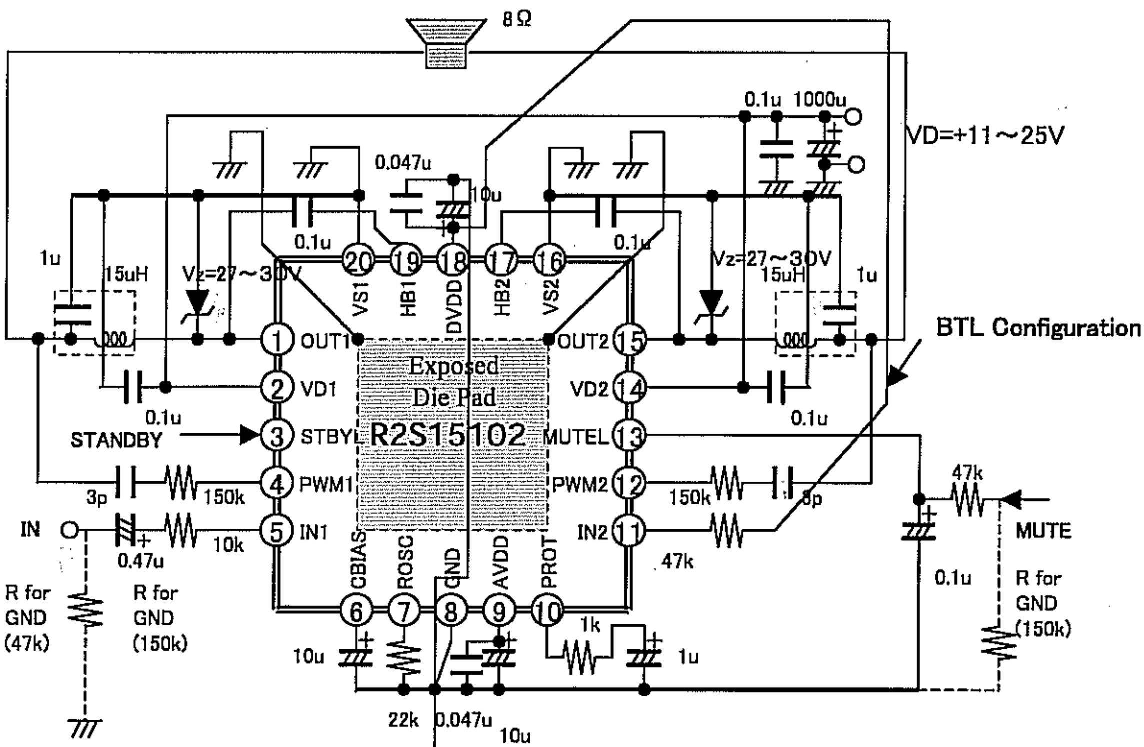
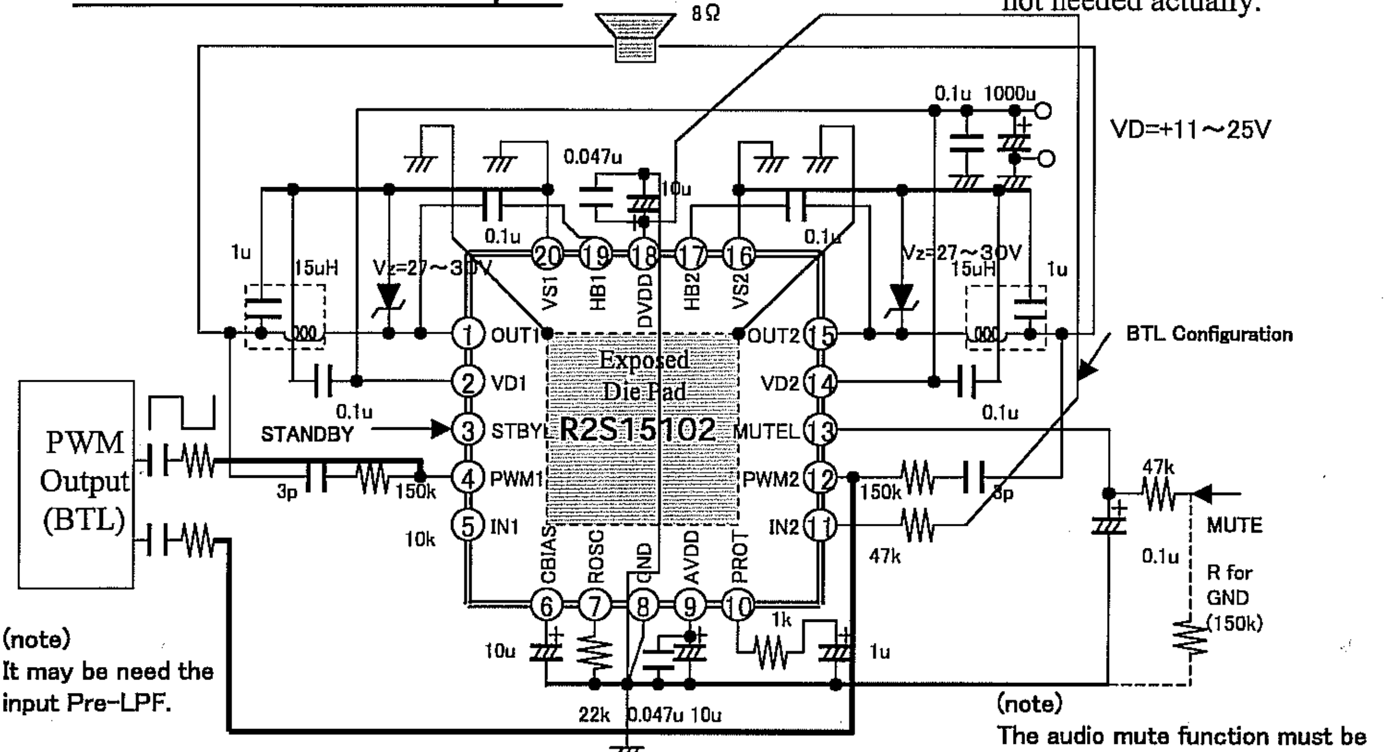


Fig.6 BTL operation mode(20W) with PWM direct input

(note)
"R for GND" 's are for the evaluation only and not needed actually.

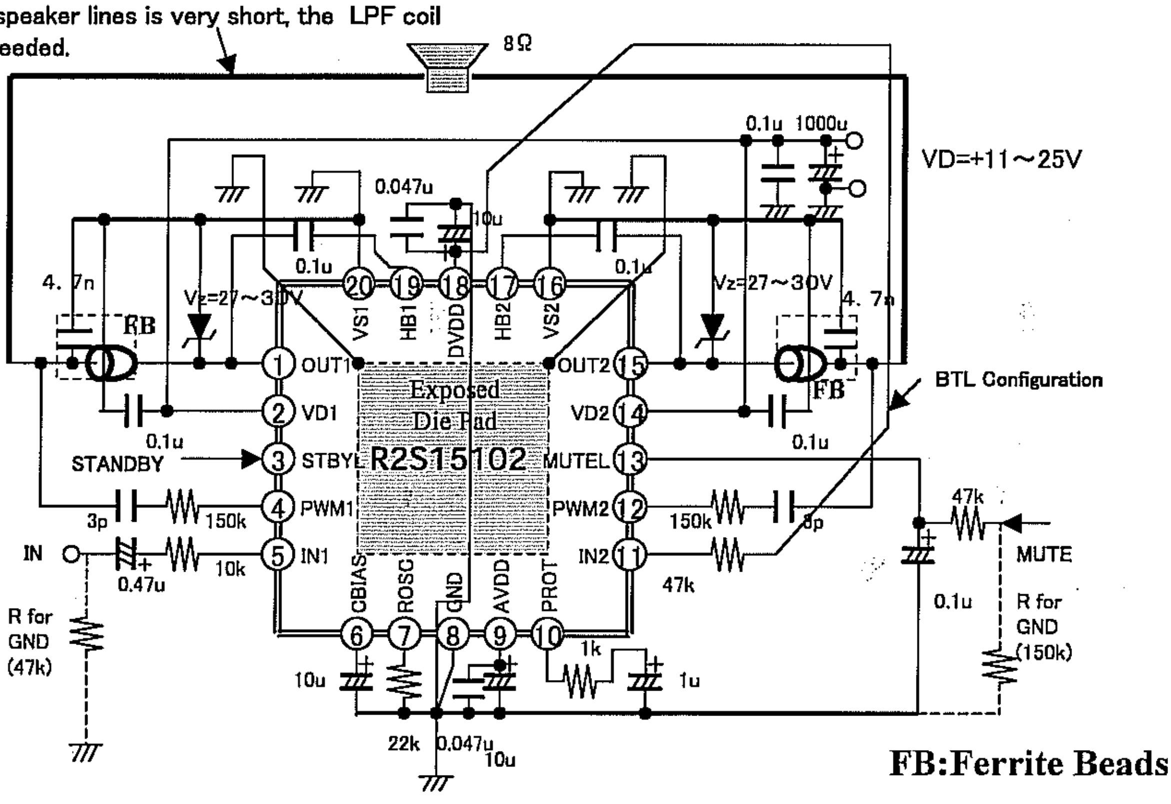


(note)
It may be need the input Pre-LPF.

(note)
The audio mute function must be done by PWM signal.

Fig.7 BTL operation mode without output LPF coil

If this speaker lines is very short, the LPF coil is not needed.



Specification
For
Approval

0. Warning and Cautions

⚠ WARNING

1) This product uses a high voltage (450 V max.). Do not touch the circuitry of this product with your hands when power is supplied to the product or immediately after turning off the power. Be sure to confirm that the voltage is dropped to a sufficiently low level.

2) Do not supply a voltage higher than that specified to this product. This may damage the product and may cause a fire.

3) Do not use this product in locations where the humidity is extremely high, where it may be splashed with water, or where flammable materials surround it. Do not install or use the product in a location that does no satisfy the specified environmental conditions. This may damage the product and may cause a fire.

4) If a foreign substance (such as water, metal, or liquid) gets inside the product, immediately turn off the power. Continuing to use the products it may cause fire or electric shock.

5) If the product emits smoke, an abnormal smell, or makes an abnormal sound, immediately turn off the power. If noting is displayed or if the display goes out during use, immediately turn off the power. Continuing to use the product as it is may cause fire or electric shock.

6) Do not disconnect or connect the connector while power to the product is on. It takes some time for the voltage to drop to a sufficiently low level after the power has been turned off. Confirm that the voltage has dropped to a safe level before disconnecting or connecting the connector. Otherwise, this may cause fire, electric shock, or malfunction.

7) Do not pull out or insert the power cable from/to an outlet with wet hands. It may cause electric shock.

8) Do not damage or modify the power cable. It may cause fire or electric shock.

9) If the power cable is damaged, or if the connector is loose, do not use the product; otherwise, this can lead to fire or electric shock.

10) If the power connector or the connector of the power cable becomes dirty or dusty, wipe it with a dry cloth. Otherwise, this can lead to fire.

CAUTION

❑ General

1) Do not place this product in a location that is subject to heavy vibration, or on an unstable surface such as an inclined surface. The product may fall off or fall over, causing injuries.
2) When moving the product, be sure to turn off the power and disconnect all the cables. While moving the product, watch your step. The product may be dropped or fall, leading to injuries of electric shock.
3) Do not place this product in a location that is subject to heavy vibration, or on an unstable surface such as an inclined surface. The product may fall off or fall over, causing injuries.
4) Before disconnecting cable from the product, be sure to turn off the power. Be sure to hold the connector when disconnecting cables. Pulling a cable with excessive force may cause the core of the cable to be exposed or break the cable, and this can lead to fire or electric shock.
5) This product should be moved by two or more persons. If one person attempts to carry this product alone, he/she may be injured.
6) This product contains glass. The glass may break, causing injuries, if shock, vibration, heat, or distortion is applied to the product.
7) The temperature of the glass surface of the display may rise to 80°C or more depending on the conditions of use. If you touch the glass inadvertently, you may be burned.
8) Do not poke or strike the glass surface of the display with a hard object. The glass may break or be scratched. If the glass breaks, you may be injured.
9) If you glass surface of the display breaks or is scratched, do not touch the broken pieces or the scratches with bare hands. You may be injured.
10) Do not place an object on the glass surface of the display. The glass may break or be scratched.

❑ Design

1) This product may be damaged if it is subject to excessive stresses (such as excessive voltage, current, or temperature). The absolute maximum ratings specify the limits of these stresses, and system design must ensure that none of the absolute maximum ratings are exceeded.
2) The materials which contain sulfur are forbidden to use, because they may damage PDP module.
3) The recommended operating conditions are conditions in which the normal operation of this product is guaranteed. All the rated values of the electrical specifications are guaranteed within these conditions. Always use the product within the range of the recommended operating conditions. Otherwise, the reliability of the product may be degraded. Use of the product with a combination of parameters, conditions, or logic not specified in the specifications of this product is not guaranteed. If intending to use the product in such a way, be sure to consult LGE in advance.
4) This product emits near infrared rays (800 to 1000nm) that may cause the remote controllers of other electric products to malfunction. To avoid this, use an infrared absorption filter and thoroughly evaluate the system and environment.

❑ **Design** (continued)

5) This product uses high-voltage switching and a high –speed clock. A system using this product should be designed so that it does not affect the other systems, and should be thoroughly evaluated.

6) This product has a glass display surface. Design your system so that excessive shock and load are not applied to the glass. Exercise care that the vent at the corner of the glass panel is not damaged. If the glass panel or vent is damaged, the product is inoperable.

7) There are some exposed components on the rear panel of this product. Touching these components may cause an electric shock.

8) This product uses a high voltage. Design your system so that any residual voltage in this product is dissipated quickly when power is turned off, observing the specifications.

9) This product uses heat-emitting components. Take the heat emitted by these components into consideration when designing your system. If the product is used outside the specified temperature range, it may malfunction.

10) This product uses a high voltage and, because of its compact design, components are densely mounted on the circuit board. If dust collects on these components, it can cause short-circuiting between the pins of the components and moisture can cause the insulation between the components to break down, causing the product to malfunction.

11) Regulations and standards on safety and electromagnetic interference differ depending on the country. Design your system in compliance with the regulations and standards of the country for which your system is intended.

12) To obtain approval under certain safety standards (such as UL and EN), a filter that passes a shock test must be fitted over the glass surface of the finished product. In addition, it must be confirmed that the level of UV emissions is within the range specified by such standards.

13) If this product is used as a display board to display a static image, "image sticking" occurs. This means that the luminance of areas of the display that remain lit for a long time drops compared with the luminance of areas that are lit for a shorter time, causing uneven luminance across the display. The degree to which this occurs is in proportion to the luminance at which the display is used. To prevent this phenomenon, therefore, avoid static images as much as possible and design your system so that it is used at a low luminance, by reducing signal level difference between bright area and less bright area through signal processing.

14) Within the warranty period, general faults that occur due to defects in components such as ICs will be rectified by LGE without charge. However, IMAGE STICKING is not included in the warranty. Repairs due to the other faults may be charged for depending on responsibility for the faults.

15) In case of AC PDP driving mechanism, Because the brightness of output is not always proportional to input signals. Therefore the non-linearity of gray can occasionally be observed in certain gray levels as well as Contour and Error Diffusion Noise can be appeared when a dark picture is on the screen especially. These are phenomena that can be observed on the PDP driving mechanism. With simple adjustment to picture brightness control, these can be reduced considerably.

16) Because of the need to control the power consumption on the PDP driving mechanism, the APL(Average Picture Level) mode was equipped. Thus, as the picture on the screen changes, there can be slightly switched in brightness. This also is a phenomenon that can be observed on the PDP driving mechanism.

17) This product is designed to LGE's "Standard" quality grade. If you wish to use the product for applications outside the scope of the "Standard" quality grade, be sure to consult LGE in advance to assess the technological feasibility before starting to design your system.

❑ USE

1) Because this product uses a high voltage, connecting or disconnecting the connectors while power is supplied to the product may cause malfunctioning. Never connect or disconnect the connectors while the power is on. Immediately after power has been turned off, a residual voltage remains in the product. Be sure to confirm that the voltage has dropped to a sufficiently low level.

2) Watching the display for a long time can tire the eyes. Take a break at appropriate intervals.

3) PDP 's brightness and contrast ratio is lower than that of the CRT. The picture is dimmer with surrounding light and better for viewing in dark condition.

4) Do not cover or wrap the product with a cloth or other covering while power is supplied to the product.

5) Before turning on power to the product, check the wiring of the product and confirm that the supply voltage is within the rated voltage range. If the wiring is wrong or if a voltage outside the rated range is applied, the product may malfunction or be damaged.

6) Do not store this product in a location where temperature and humidity are high. This may cause the product to malfunction.

7) If the glass surface of the display becomes dirty, wipe it with a soft cloth moistened with a neutral detergent. Do not use acidic or alkaline liquids, or organic solvents.

8) Do not tilt or turn upside down while the module package is carried, the product may be damaged.

9) This product is made from various materials such as glass, metal, and plastic. When discarding it, be sure to contact a professional waste disposal operator.

❑ Repair and Maintenance

Because this product combines the display panel and driver circuits in a single module, it cannot be repaired or maintained at user's office or plant. Arrangements for maintenance and repair will be determined later

❑ Others

1) If your system requires the user to observe any particular precautions, in addition to the above warnings and cautions, include such caution and warning statements in the manual for your system.

2) If you have any questions concerning design, such as on housing, storage, or operating environment, consult LGE in advance.

1. GENERAL DESCRIPTION

❑ DESCRIPTION

The PDP42X2##2# 42-inch 16:9 color plasma display module with resolution of 1024(H) × 768(V) pixels. This is the display device which offers vivid colors with adopting AC plasma technology by LG Electronics Inc.

❑ FEARURES

High peak brightness (1,000cd/m^2 Typical) and high contrast ratio (5,000:1 Typical) enables user to create high performance PDP SETs.

❑ APPLICATIONS

- ✓ Public information display
- ✓ Video conference systems
- ✓ Education and training systems



❑ ELECTRICAL INTERFACE OF PLASMA DISPLAY

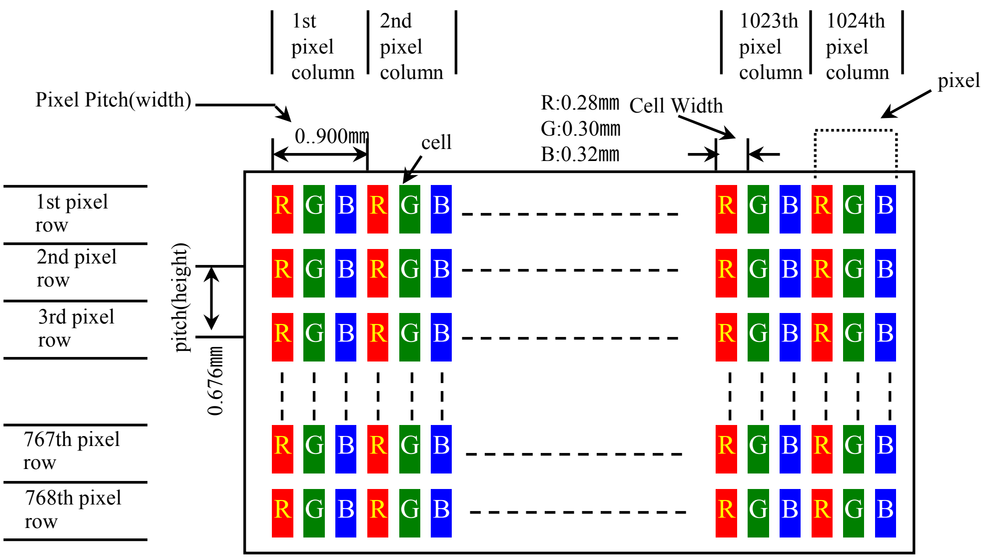
The PDP42X2#### requires 8bits or 10bits of digital video signals for each RGB color.
This is the display device which offers vivid colors with adopting AC plasma technology by LG Electronics Inc.

❑ GENERAL SPECFICATIONS

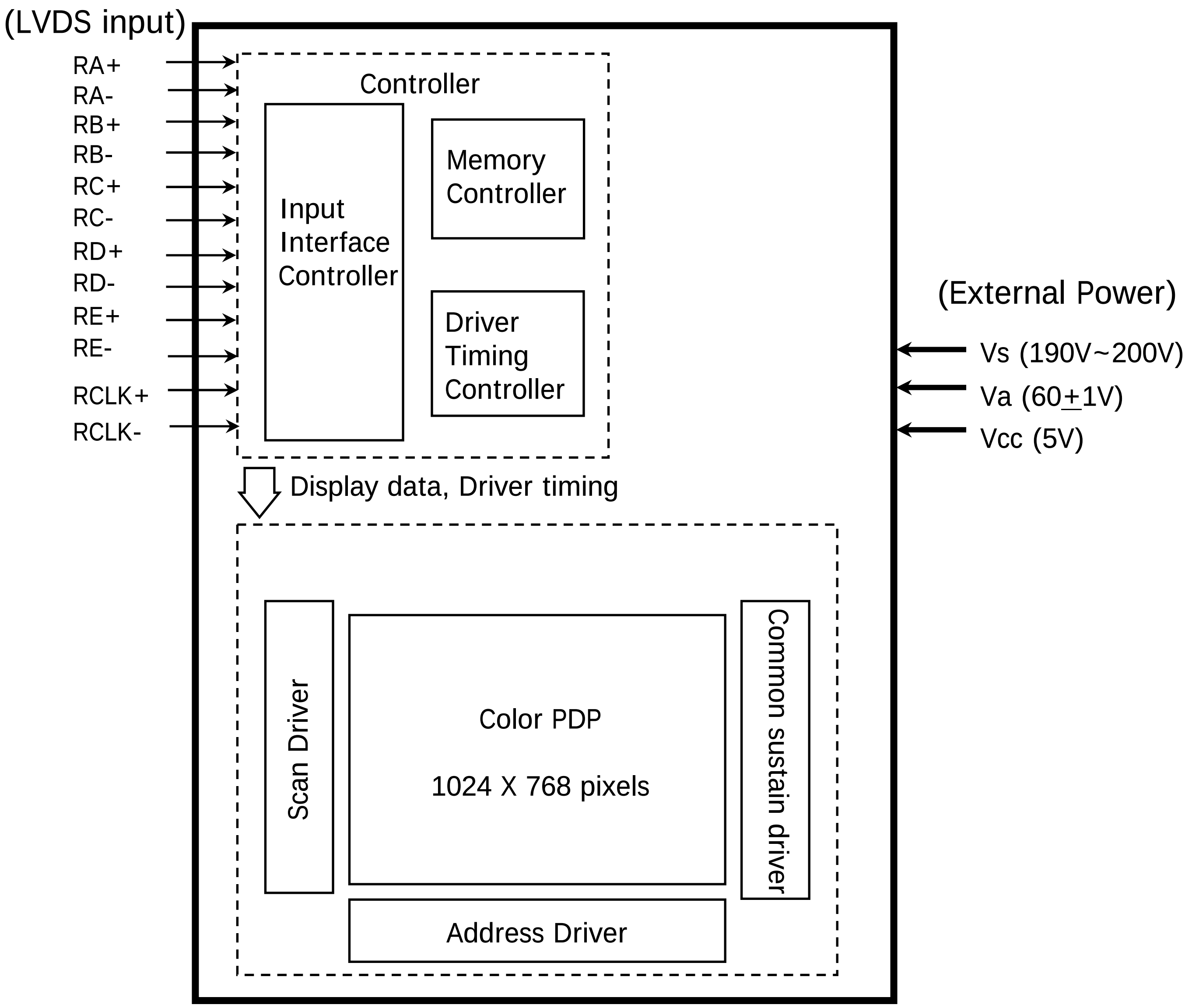
✓ Model Name : PDP42X2#### (42X2A Model)
✓ Number of Pixels : 1024(H) × 768(V) (1pixel=3 RGB cells)
✓ Pixel Pitch : 900µm (H) × 676µm (V)
✓ Cell Pitch : 300µm (H) × 676µm (V) (Green Cell basis)
✓ Display Area : 920.1(H) × 518.4(V) ±0.5mm
✓ Outline Dimension : 1005(H) × 597(V) × 60.7(D)±1mm
✓ Pixel Type : RGB Closed type
✓ Number of Gradations: (R)1024 × (G)1024 × (B)1024
✓ Weight : 15.3 Kg ± 0.5 Kg (Net 1EA)
113.5 Kg ± 5 Kg (5EA/1BOX)
✓ Aspect Ratio : 16:9
✓ Peak Brightness : Typical 1000cd/㎡ (1/100 White Window)
✓ Contrast Ratio : Typical 50:1 (In a bright room with 150Lux at center)
: Typical 5000:1 (In a dark room 1/100 White Window pattern at center)
✓ Power Consumption : Typical 280 W (Full White), Max.330W
✓ Expected Life-time : more than 60,000 Hours of continuous operation

☞ Life-time is defined as the time when the brightness level becomes half of its initial value.

✓ Display Dot Diagram



❑ BLOCK DIAGRAM



☞ Applied Voltage level is specified at the time when Full-White pattern is displayed on the panel.

Item	Symbol	Condition	Min.	Max.	Unit	Remarks
Logic Voltage	Vcc	25°C	4.5	6	V	
Address Voltage	Va	25°C	-	70	V	
Sustain Voltage	Vs	25°C	-	220	V	

Item	Condition	Min.	Typ.	Max.	Unit
Adjustable Range	-	4.75	5.0	5.25	V
Voltage Stability	-	-	-	±3.0	%
Average Current	-	1	4.5	5.5	A_{mean}
Peak Current	-	-	-	8.5	A
Ripple	-	-	-	30	mV_{p-p}
Noise	-	-	-	300	mV_{p-p}

Item	Condition & Remarks	Min.	Typ.	Max.	Unit

➢ Sustain Power Supply(Vs)

Item	Condition	Min.	Typ.	Max.	Unit
Adjustable Range	Dependent on the characteristics of each PDP	190	-	200	V
Voltage Stability	-	-	-	±1.0	%
Peak Current	-	-	-	20	A
Average Current	Dependent on the characteristics of each PDP	0.1	-	1.5	A_{mean}
Voltage Regulation	At the peak current	-	-	3	V
Ripple & Noise	-	-	-	500	mV_{p-p}

☞ Voltage should be set to a specified value which is indicated on the label attached to the module.

❑ Insulation

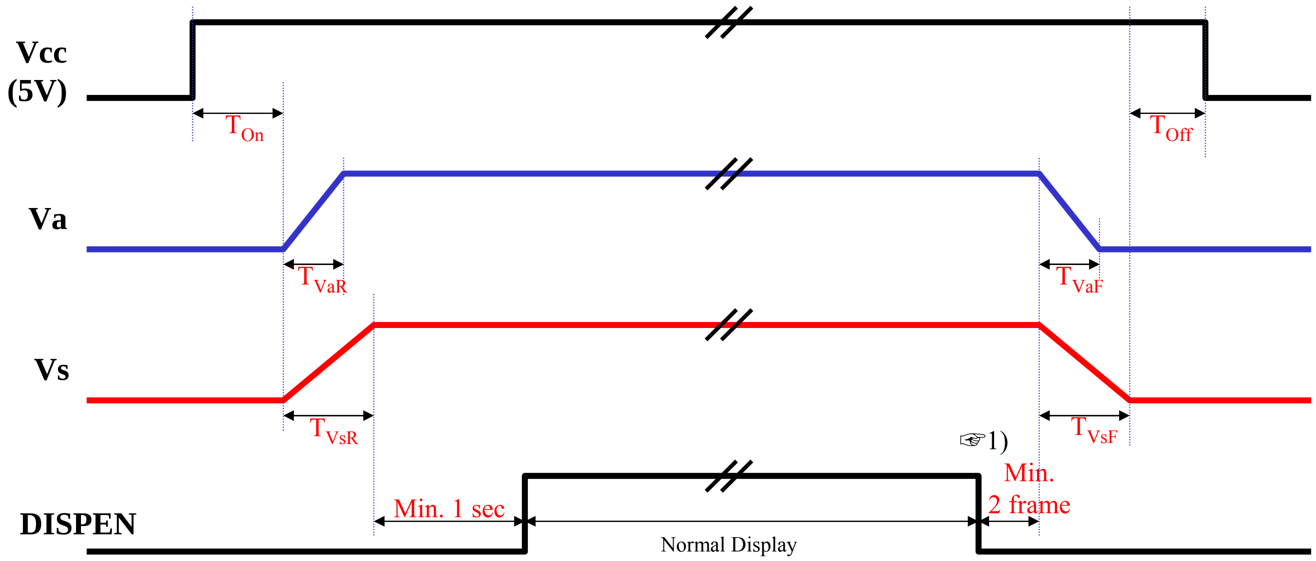
- In order to use information technology equipment, the end-user product should satisfy the insulation and material requirements on Safety Standards of IEC 60950, EN 60950, UL60950 and CSA C22.2 No 60950, or IEC 60065, EN 60065, UL 6500 and CSA C22.2 No 60065

- The screen filter(Black mask filter) of end-user products should satisfy the supplementary insulation.

❑ Additional requirements

- Proper fire enclosure
- Proper mechanical enclosure
- Safety test including Power Supply Board should be performed as a part of the end-user product investigation.

❑ Power Supply Sequence



Symbol	Description	Min.	Max.	unit
T_{On}	Time interval between 90% of Vcc and 10% of Vs when Power On	0.2	-	sec
T_{Off}	Time interval between 10% of Vs and 90% of Vcc when Power Off	300	-	ms
T_{VaR}	Rising Time of Va (10% to 90%)	**100**	**300**	ms
T_{VaF}	Falling Time of Va (90% to 10%)	**100**	**300**	ms
T_{VsR}	Rising Time of Vs (10% to 90%)	**150**	800	ms
T_{VsF}	Falling Time of Vs (90% to 10%)	**150**	500	ms

☞ If power sequence does not meet to above sequence diagram, PDP drivers may be damaged permanently.
☞ Even when AC input power supply is switched ON/OFF, above sequence should be observed strictly.
☞1) We recommend that it will be used this data (Min.2 frame) because of reducing image-sticking.

❑ LVDS Signal

➢ Definitions and Functions of LVDS Signal

Symbol	Definition and Function	Related Output Signal
RA＋	Channel-A Pos. Receiver Input	R4, R5, R6, R7, R8, R9, G4
RA－	Channel-A Neg. Receiver Input	
RB＋	Channel-B Pos. Receiver Input	G5, G6, G7, G8, G9, B4, B5
RB－	Channel-B Neg. Receiver Input	
RC＋	Channel-C Pos. Receiver Input	B6, B7, B8, B9, $\overline{\text{Hsync}}$, $\overline{\text{Vsync}}$, $\overline{\text{BLANK}}$
RC－	Channel-C Neg. Receiver Input	
RD＋	Channel-D Pos. Receiver Input	R2, R3, G2, G3, B2, B3
RD－	Channel-D Neg. Receiver Input	
RE ＋	Channel-E Pos. Receiver Input	R0, R1, G0, G1, B0, B1
RE －	Channel-E Neg. Receiver Input	
RCLK＋	Clock Pos. Receiver Input	PIX_CLK
RCLK－	Clock Neg. Receiver Input	

➢ Video Input Connector (P31)

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	GND	11	RD-	21	nc
2	RA-	12	RD+	22	nc
3	RA+	13	GND	23	nc
4	RB-	14	GND	24	RE-
5	RB+	15	nc	25	RE+
6	GND	16	nc	26	
7	RC-	17	nc	27	
8	RC+	18	nc	28	
9	RCLK-	19	GND	29	
10	RCLK+	20	nc	30	
				31	

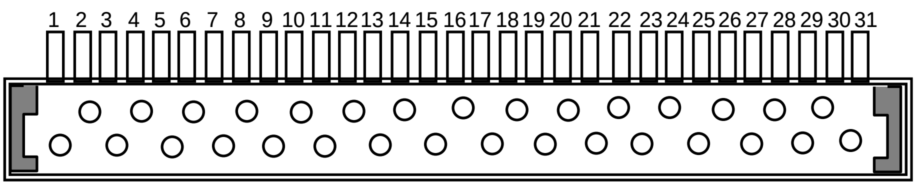
(Pins 27–29: 3.3V level)

* DISPEN need to be set to “LOW” when power is ON and OFF, need to be set to “HIGH” when normal operation.

☞ According to the PDP Module Gamma Mode, ths RGB video sginal can be changed.

☞ Twisted pair cable must be used for LVDS signal

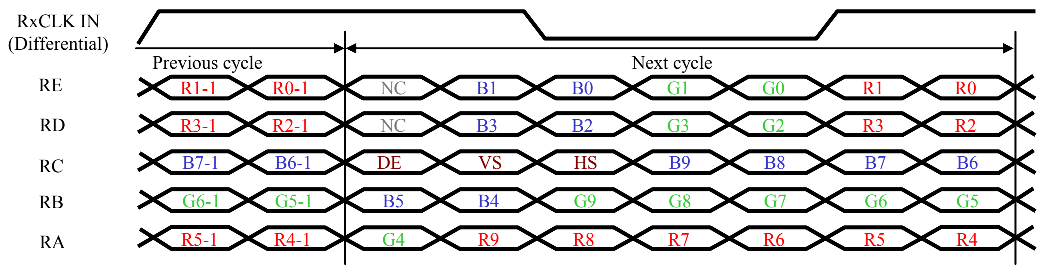
☞ Default 8 bit input (For 10 bit input, ROM should be changed)



LG Cable, GT121-31P-TD pin number (Top view)

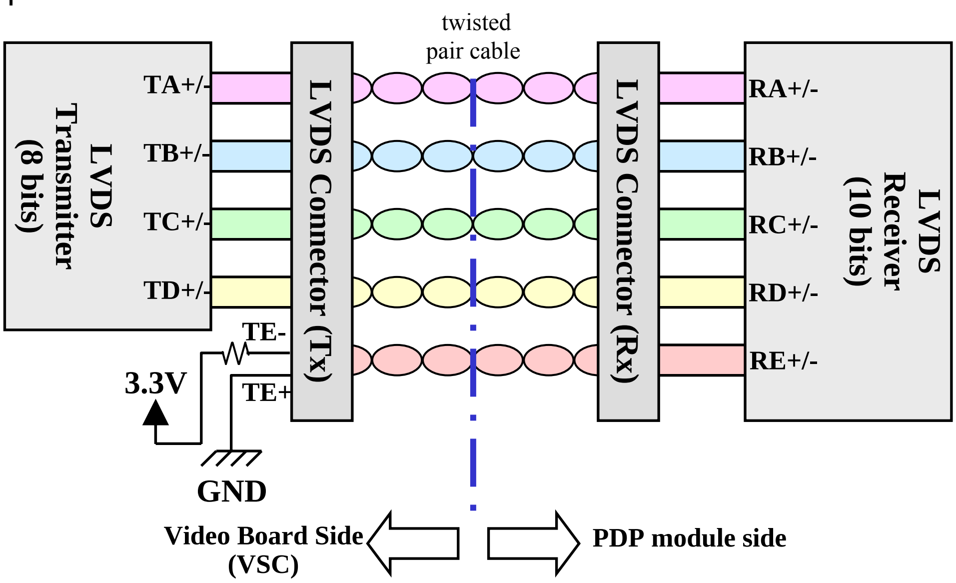
❑ **LVDS Signal** (continued)

➢ Signal Input sequence of LVDS Receiver



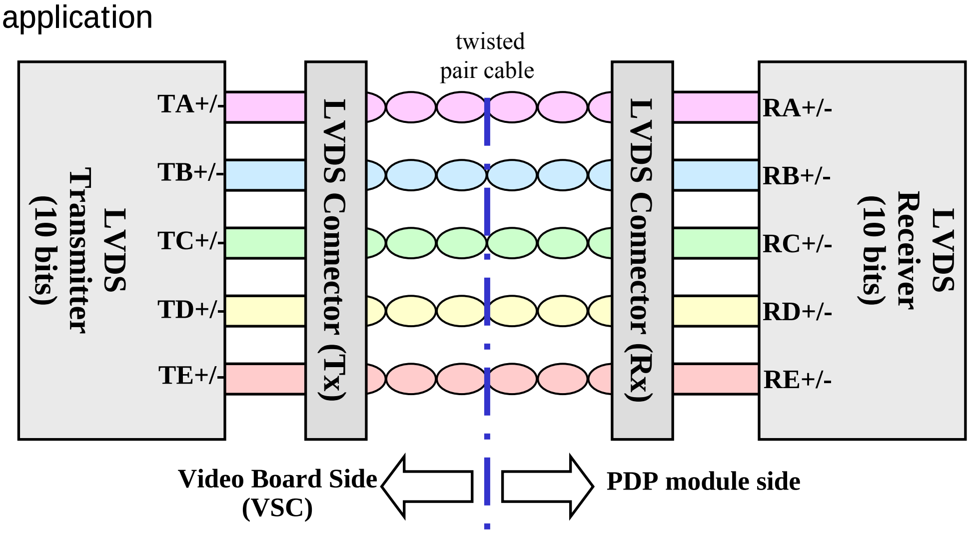
※ DE : BLANK, VS : Vsync, HS : Hsync

➢ 8bit application

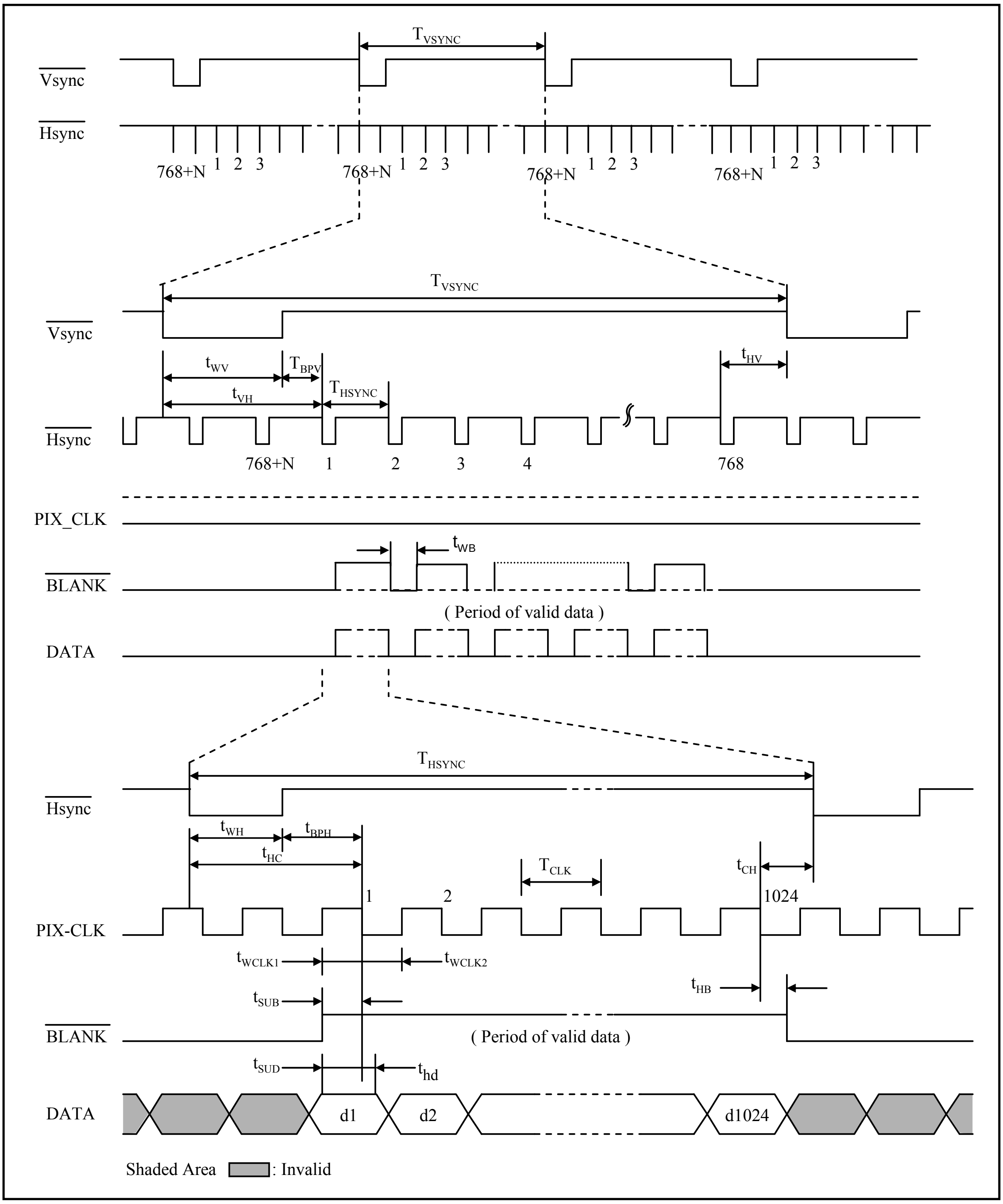


※ To use (only) 8bit video signal, “TE+” is to be tied to ground signal and “TE-” is to be tied to 3.3V signal. (to set the 2 LSB of 10 bits video signal to ‘0’)

➢ 10bit application



☞ Default 8 bit input (For 10 bit input, it need to discuss with PDP Division)



☞ T_{WB} must be larger than 4.6μs

❑ Input Signal Timing Specification

➢ 60Hz Mode

No.	Symbol	Min.	Typ.	Max.	Unit	Remark
1	T_{vsync}	16.604 (803H)	16.666 (806H)	16.728 (809H)	ms (H)	1 frame = 59.8Hz ~ 60.2Hz
2	t_{wv}	84 (4H)	124 (6H)	168 (8H)	µs (H)	
3	t_{vh}	357 (17H)	413(20H)	483(23H)	µs (H)	
4	t_{hv}	-	372(18H)	-	µs (H)	
5	T_{hsync}	20.62 (1340D)	20.68 (1344D)	20.74 (1348D)	µs (D)	
6	t_{wh}	2.03(132D)	2.09(136D)	2.15(140D)	µs (D)	
7	t_{hc}	4.49 (292D)	4.55(296D)	4.62(300D)	µs (D)	
8	t_{ch}	-	0.37(24D)	-	µs (D)	
9	t_{clk}	15.2 (65.8MHz)	15.4 (65MHz)	15.6 (64MHz)	ns	$t_{clk} = t_{wclk1} + t_{wclk2}$
10	t_{wclk1}	-	7.7	-	ns	
11	t_{wclk2}	-	7.7	-	ns	
12	t_{sub}	-	7.7	-	ns	$t_{sub} \leq t_{hc}$
13	t_{hb}	-	7.7	-	ns	$t_{hb} \leq t_{ch}$
14	t_{sud}	-	7.7	-	ns	
15	t_{hd}	-	7.7	-	ns	

☞ Note
1. Min. & Max. of each signal is measured value when other signal is Typ.
2. When changing V_{SYNC} & H_{SYNC} Timing, it is recommended to vary it with even multiple of H & D.
3. T_{WB} must be larger than 4.6µs.

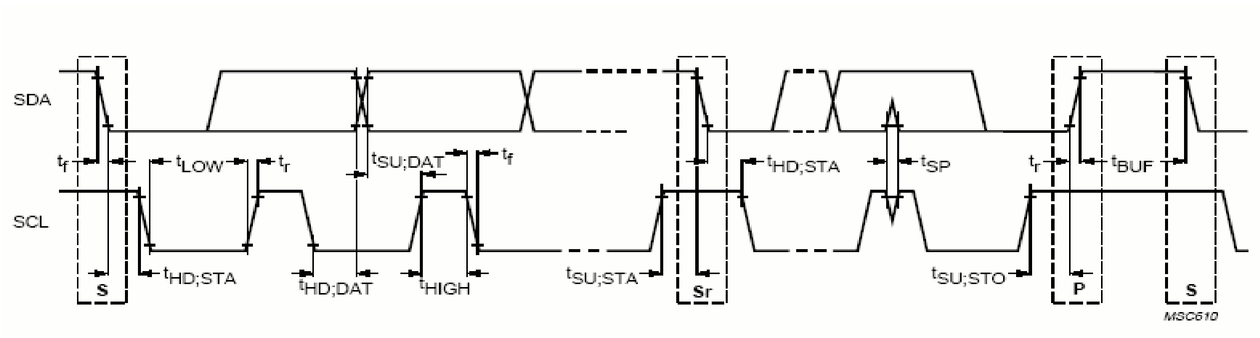
❑ Input Signal Timing Specification (Continued)

➢ 50Hz Mode

No.	Symbol	Min.	Typ.	Max.	Unit	Remark
1	T_{vsync}	19.850 (960H)	19.995 (967H)	20.139 (974H)	ms (H)	1 frame = 49.65Hz ~ 50.38Hz
2	t_{wv}	84 (4H)	124 (6H)	168 (8H)	µs (H)	
3	t_{vh}	357 (17H)	413(20H)	483(23H)	µs (H)	
4	t_{hv}	-	3759(179H)	-	µs (H)	
5	T_{hsync}	20.62 (1340D)	20.68 (1344D)	20.74 (1348D)	µs (D)	
6	t_{wh}	2.03(132D)	2.09(136D)	2.15(140D)	µs (D)	
7	t_{hc}	4.49 (292D)	4.55(296D)	4.62(300D)	µs (D)	
8	t_{ch}	-	0.37(24D)	-	µs (D)	
9	t_{clk}	15.2 (65.8MHz)	15.4 (65MHz)	15.6 (64MHz)	ns	$t_{clk} = t_{wclk1} + t_{wclk2}$
10	t_{wclk1}	-	7.7	-	ns	
11	t_{wclk2}	-	7.7	-	ns	
12	t_{sub}	-	7.7	-	ns	$t_{sub} \leq t_{hc}$
13	t_{hb}	-	7.7	-	ns	$t_{hb} \leq t_{ch}$
14	t_{sud}	-	7.7	-	ns	
15	t_{hd}	-	7.7	-	ns	

☞ Note

1. Min. & Max. of each signal is measured value when other signal is Typ.
2. When changing V_{SYNC} & H_{SYNC} Timing, it is recommended to vary it with even-multiple of H & D.
3. T_{WB} must be larger than 4.6µs.



PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	μs
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	μs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	μs
Data hold time: for CBUS compatible masters (see NOTE, Section 10.1.3) for I²C-bus devices	$t_{HD;DAT}$	5.0 0(2)	– 3.45(3)	– 0(2)	– 0.9(3)	μs μs
Data set-up time	$t_{SU;DAT}$	250	–	100(4)	–	ns
Rise time of both SDA and SCL signals	t_r	–	1000	20 + 0.1C_b(5)	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	20 + 0.1C_b(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	μs
Capacitive load for each bus line	C_b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	0.1V_{DD}	–	0.1V_{DD}	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	0.2V_{DD}	–	0.2V_{DD}	–	V

Notes

1. All values referred to V_{IHmin} and V_{ILmax} levels (see Table 4).
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\,max}$ + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released.
5. C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times according to Table 6 are allowed.

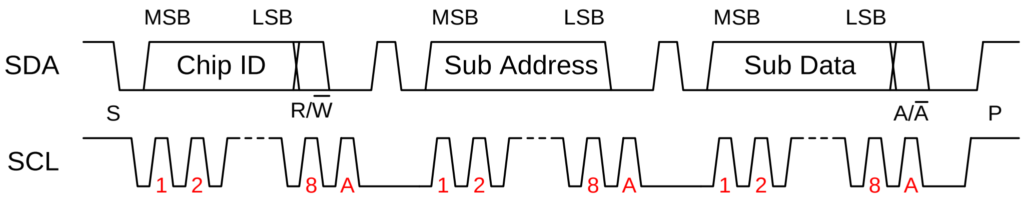
n/a = not applicable

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
LOW level input voltage: fixed input levels V_{DD}-related input levels	V_{IL}	 −0.5 −0.5	 1.5 $0.3V_{DD}$	 n/a −0.5	 n/a $0.3V_{DD}$ [1]	 V V
HIGH level input voltage: fixed input levels V_{DD}-related input levels	V_{IH}	 3.0 $0.7V_{DD}$	 [2] [2]	 n/a $0.7V_{DD}$ [1]	 n/a [2]	 V V
Hysteresis of Schmitt trigger inputs: $V_{DD} > 2$ V $V_{DD} < 2$ V	V_{hys}	 n/a n/a	 n/a n/a	 $0.05V_{DD}$ $0.1V_{DD}$	 – –	 V V
LOW level output voltage (open drain or open collector) at 3 mA sink current: $V_{DD} > 2$ V $V_{DD} < 2$ V	 V_{OL1} V_{OL3}	 0 n/a	 0.4 n/a	 0 0	 0.4 $0.2V_{DD}$	 V V
Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10 pF to 400 pF	t_{of}	–	250 [4]	$20 + 0.1C_b$ [3]	250 [4]	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	n/a	n/a	0	50	ns
Input current each I/O pin with an input voltage between $0.1V_{DD}$ and $0.9V_{DDmax}$	I_i	−10	10	−10 [5]	10 [5]	µA
Capacitance for each I/O pin	C_i	–	10	–	10	pF

Notes

1. Devices that use non-standard supply voltages which do not conform to the intended I²C-bus system levels must relate their input levels to the V_{DD} voltage to which the pull-up resistors R_p are connected.
2. Maximum $V_{IH} = V_{DDmax} + 0.5$ V.
3. C_b = capacitance of one bus line in pF.
4. The maximum t_f for the SDA and SCL bus lines quoted in Table 5 (300 ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_s) to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in Fig.36 without exceeding the maximum specified t_f.
5. I/O pins of Fast-mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.

n/a = not applicable



☞ First 1byte data must be 0001 1100 (0x1C) ← last 1bit is 0(write mode).

❑ I²C Register Description

➢ I²C Register Brief

R : Reserved(don't care)

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x01	Sync Mode Registers							
	R	R	R	R	R	sync_auto	0	hz_select
0x08	Bright Mode Registers							
	br_mode_50(1:0)		br_mode60(1:0)		0	0	0	0
0x09	Power Save Mode Registers							
	R	R	ps_mode_50(2:0)			ps_mode_60(2:0)		
0x0B	Gamma Mode Registers							
	gamma_50(1:0)		gamma_60(1:0)		0	0	0	0
0x10	Color Inversion Registers							
	R	R	R	R	R	R	R	Bw_inv_sw
0x11	Scroll Register							
	R	R	R	R	R	scroll_mode_sw	scroll_mode(1:0)	
0x18	ISM Mode Registers							
	R	R	R	R	R	ism_mode	R	R

❑ I²C Register Description

● Sync Mode Registers

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x01	Sync Mode Registers							
	R	R	R	R	R	sync_auto	0	hz_select
Default	R	R	R	R	R	1	0	0

• sync_auto : Sync automatic / manual mode selection
1:auto, 0:manual
• hz_select : Frequency mode selection
0 : 50Hz, 1 : 60Hz
When the sync_auto is "high", hz_select is ignored.

Manual Mode(sync_auto = 0)

hz_select	Function
0	Display only 50Hz
1	Display only 60Hz

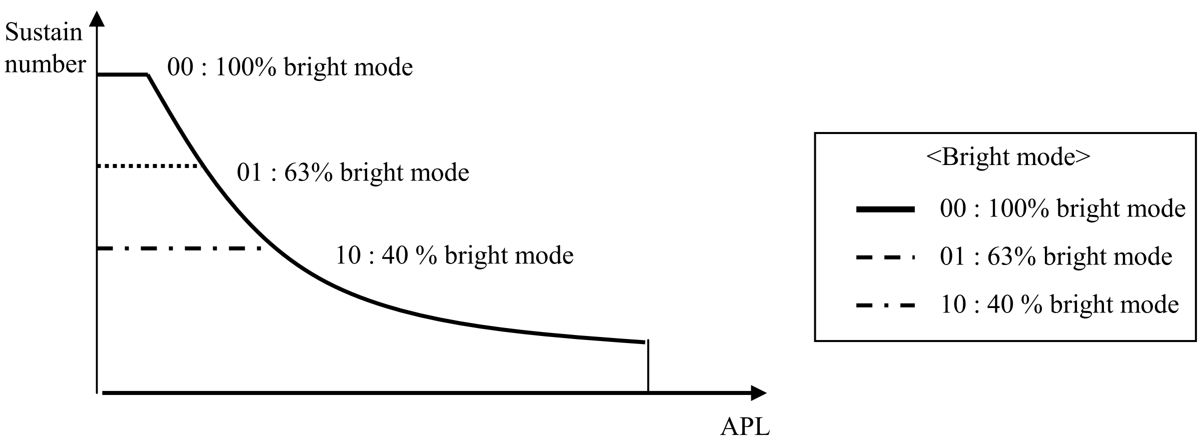
Auto Mode (sync_auto = 1)

hz_select	Function
Don't care	50Hz, 60Hz automatic conversion

● Bright Mode Registers

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x08	Bright Mode Registers							
	br_mode_50av(1:0)		br_mode60av(1:0)		R	R	R	R
Default	0	0	0	0	R	R	R	R

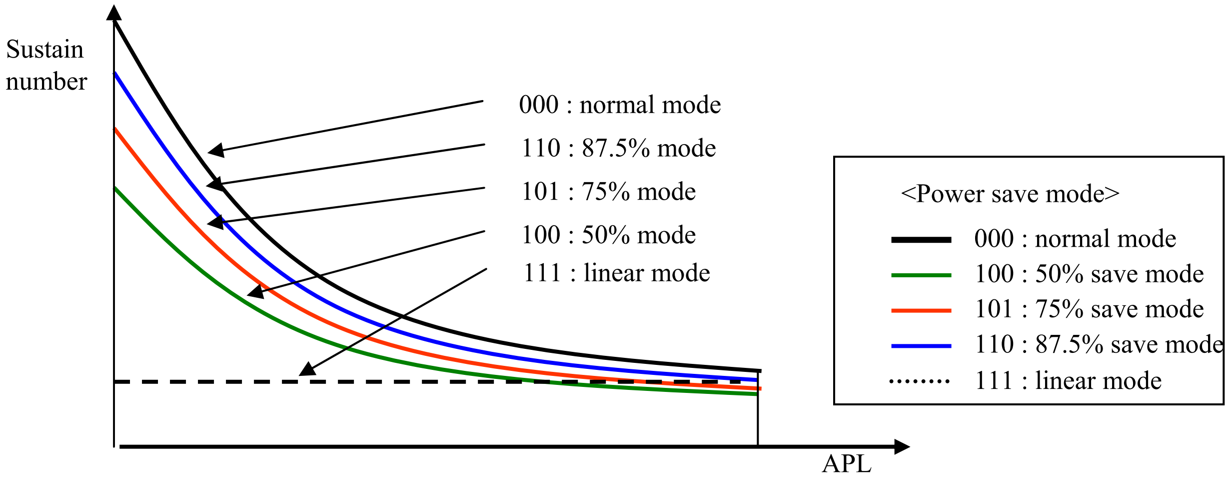
• br_mode_50(1:0) : Bright mode for 50Hz
• br_mode_60(1:0) : Bright mode for 60Hz



● Power Save Mode Registers

I^{2}C Addr.	I^{2}C Data							
	7	6	5	4	3	2	1	0
0x09	Power Save Mode Registers							
	R	R	ps_mode_50(2:0)			ps_mode_60(2:0)		
Default	R	R	0	0	0	0	0	0

- ps_mode_50(2:0) : Power save mode for 50Hz
- ps_mode_60(2:0) : Power save mode for 60Hz



Power save / Bright	100%	87.5%	75%	50%
100%	⦿	⦿	△	△
63%	⦿	⦿	⦿	△
40%	⦿	⦿	⦿	⦿

⦿ - recommneded, △- not recommended

☞ In case of “Not Recommended”, there are no problems related reliability but it may cause a flicker on the screen because of sudden change of sustain number.

● Gamma Mode Registers

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x0B	Gamma Mode Registers							
	gamma_50(1:0)		gamma_60(1:0)		R		R	
Default	0	0	0	0	R		R	

• gamma_50(1:0) : Gamma mode for 50Hz
• gamma_60(1:0) : Gamma mode for 60Hz

Value	Table#	Contents of table
00	Gamma A	Γ = N 2.2 for R, G, B
01	Gamma B	Γ = N 1.0 for R, G, B
10	Gamma C	Γ = reserved
11	Gamma D	Γ = Reserved

● Color Inversion Registers

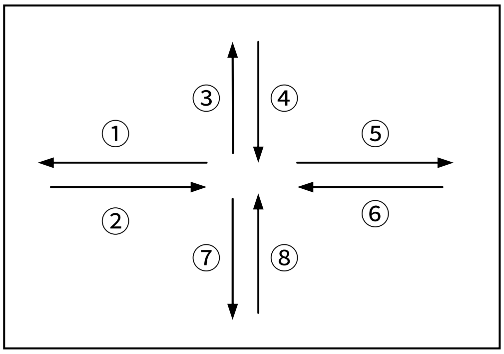
I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x10	Color Inversion Registers							
	R	R	R	R	R	R	R	Bw_inv_sw
Default	R	R	R	R	R	R	R	0

• Image inversion enable signal for preventing image sticking.
• bw_inv_sw : picture Color Inversion (1:ON, 0:OFF) ➔ default : 0

● Scroll Registers

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x11	Scroll Register							
	R	R	R	R	R	scroll_ mode_sw	scroll_mode(1:0)	
Default	R	R	R	R	R	0	1	1

• Picture scrolling enable signal for preventing image sticking.
• scroll_mode_sw : Scroll mode switch (1:ON, 0:OFF) ➔ default : 0
• scroll_mode[1] : horizontal scroll ON/OFF (1:ON, 0:OFF) ➔ default : 1
• scroll_mode[0] : vertical scroll ON/OFF (1:ON, 0:OFF) ➔ default : 1



※ Scroll procedure

☞ ①(C→L) ②(L→C) ③(C→U) ④(U→C)
⑤(C→R) ⑥(R→C) ⑦(C→D) ⑧(D→C)
※ C:Center, L:Left, R:Right, U:Up, D:Down

☞ When "scroll" is OFF during scrolling,
SCROLL operation is stopped after the screen is returned to the original position(center).

● ISM Mode Registers

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x18	ISM Mode Registers							
	R	R	R	R	R	Ism_mode	1	1
Default	R	R	R	R	R	1	1	1

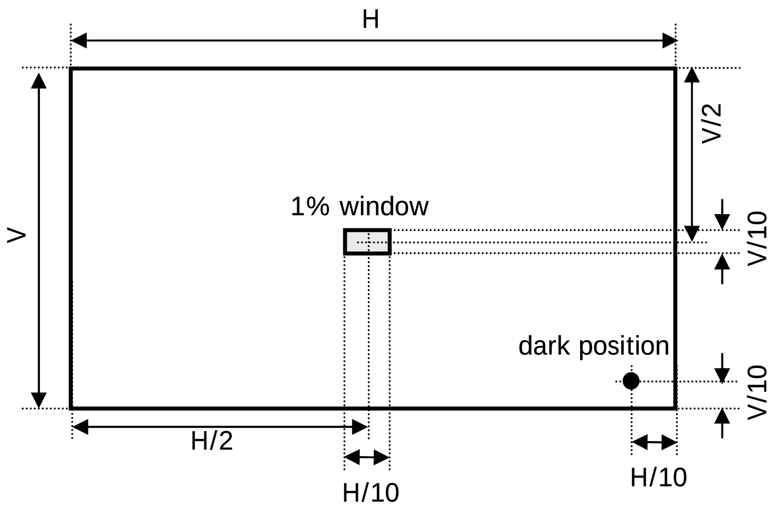
• ims_mode : ISM mode switch (1: ON, 0:OFF)

3. ELECTRO OPTICAL SPECIFICATIONS

❑ Electro Optical characteristic Specifications (60Hz)

ITEM	Symbol	Condition ☞1)	Min	Typ	Max	Unit
Peak White Brightness*	B_{WP}	1% white window	700	1,000	-	cd/m^2 ☞2)
Average White Brightness*	B_W	Full White	160	200	-	cd/m^2
Brightness Uniformity	B_U	Full White	-10	0	+10	
Color Coordinate, White, X	X_W	Full White	0.280	0.300	0.320	
Color Coordinate, White, Y	Y_W	Full White	0.290	0.310	0.330	
Color Coordinate Uniformity	C_U	Full White	-0.01	average	+0.01	
Contrast Ratio*, Bright Room	CR_{BR}	150Lx at center	-	50:1	-	☞2)
Contrast Ratio*, Dark Room ☞3)	CR_{DR}	1% white window	3000:1	5,000:1	-	☞2)
Brightness Difference	Bd	Test pattern for Bd			25	cd/m2
Power Consumption ☞4)	P_W	Full White	-	280	330	

☞*) Peak brightness & contrast ratio at 50Hz is about 80% level of 60Hz data.
☞1) All characteristics are measured in the normal temperature in the normal ambient temperature.
☞2) The brightness of the white peak position is measured while the 1%-window pattern is "ON" state. And then, it should be measured in 10 seconds after 1%-window is "ON" state.
➔ For the measurement position, refer to the following figure.
☞3) The brightness of dark room should be less than 1 lux.
☞4) Total Power Consumption can be upto 350W according to the displayed pattern.

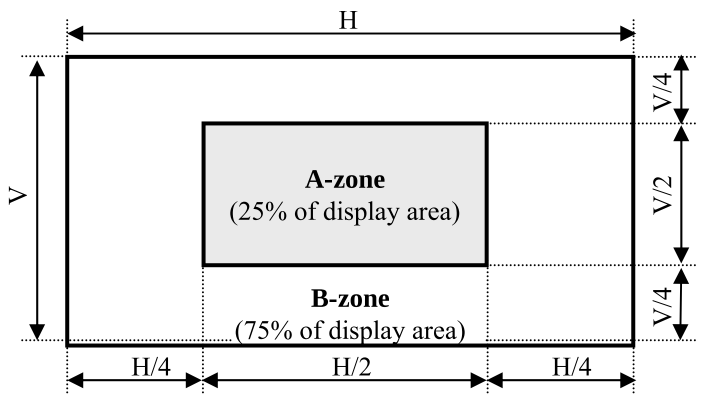


❑ Cell Defect Specifications

Defect	Specification		
	Number of Cell Defects (N)		Distance between two defects (D)
Non-Ignition Dot ☞1) + Unstable Dot ☞2)	A-zone	▶Total N ≤ 4[cells / full screen] ▶ N ≤ 2 [cells / each R,G,B screen] ▶ N = 0 [adjacency of 2-cells / full-white screen]	▶A-Zone : ≥ 100mm ▶B-Zone : N≤2 (100mm Circle/screen:2points allowed) ▶A, B Zone overlap:N≤2 (100mm Circle/screen:2points allowed)
	B-zone	▶ Total N ≤ 11 [cells / full screen] ▶ N ≤ 5 [cells / each R,G,B screen] ▶ N ≤ 2 [adjacency of 2-cells / full-white screen] = 0 [adjacency of 3-cells / full-white screen]	
Uncontrollable Dot ☞3)	A-zone	▶ N ≤ 1 [cells / cells/each R,G,B screen]	
	B-zone	▶ Total N ≤ 3 [cells / full screen]	
Non-Extinguishing Dot ☞4)	A-zone	▶ N = 0	
	B-zone	▶ N = 0	
▶ Total sum of all defects N ≤ 17 [cells / full-white screen]			
Stain ☞5)	▶ N ≤ 6 , for the stain of which longer-axis length is 5mm or shorter. ▶ N =0 , for the stain of which longer-axis length is longer than 5mm.		▶ D ≥ 50 mm

☞**1) Non-Ignition Dot**(Dark Defect) is defined as "A cell of which more than 50% area is not ignited"
☞**2) Unstable Dot** (Flickering) is defined as "A cell which repeats On and Off"
☞**3) Uncontrollable Dot** is defined as "A cell which is distinctly brighter or darker than other cells around it" and/or "A cell of which color is distinctly different from that of other cells around it"
☞**4) Non-Extinguishing Dot** (brightness defect) is defined as "A cell of which more than 50% area is always ON"
☞**5) Stain** is defined as "A blob due to local color contamination in white or simple color pattern"

* The decision distance is 3H away from the panel, intensity of illumination is between 100 Lux and 200 Lux.



4. MECHANICAL & ENVIRONMENTAL SPECIFICATIONS

❑ Mechanical Characteristic Specifications

Item		Spec.	Unit	Remark
Outline Dimensions		1,005(H) × 597(V) × 61.2(D) ± 1	mm	See "Outline Drawing"
Display Area		920.1 (H) x 518.4 (V) ± 0.5	mm	
Weight	Net	15.3 ± 0.5 (1EA)	kg	
	Gross	113.5 ± 5 (5EA/1BOX)	kg	

❑ Vibration and Drop Specifications

Item	Condition	Remark
Vibration	Non-Operational (5ea Packed state)	1.25G, 5 to 55Hz (Sweep time : 2Min) Y direction, 60minutes
Drop (5ea Packed state)	Bottom	Free Falling : 30cm
	The rest (Front, Backside)	Inclined : 20-25cm

❑ Recommended Environmental Conditions

Item		Condition	Remark
Ambient Temperature	Operation	0°Cto 40°C	Panel surface temperature must be kept less than 70 °Cfor normal operation.
	Storage	-20°C to 60°C	
Humidity	Operation	20 to 80% RH	No condensation
	Storage	10 to 90% RH	
Air Pressure	Operation	800 to 1,100 hPa	0~2000m above the sea level
	Storage	700 to 1,100 hPa	0~3000m above the sea level

5. IMAGE STICKING CHARACTERISTICS

❑ Image Sticking

The fluorescent substance used in the plasma module loses its brightness with the lapse of lighting time. This deterioration in brightness appears to be a difference in brightness in relation to the surroundings, and comes to be recognized as image sticking.

In other words, the image sticking is defined as follows: when the same pattern (of the fixed display) is displayed for a long time, a difference in brightness is caused around the lighting area and non-lighting area due to deterioration in the fluorescent substance.

When the present pattern is changed over to another one, the boundary comes to be seen between the lighting area and non-lighting area due to difference in brightness in the pattern shown shortly before changeover. If this conditions is accumulated, the boundary or image sticking comes to be seen with the naked eyes.

❑ Secular change in brightness

The life of brightness, defined as the reduction to half the initial level, is more than 25 thousand hours on average.

Conditions: All white (100% white) input at an ambient temperature of 25°C.

However, this lifetime is not a guarantee value for life and brightness. It should be recognized simply as the data for reference.

❑ Warranty

Image sticking and faults in brightness and picture elements are excluded from the warranty objects.

❑ Cause of deterioration in brightness

A major possible cause of deterioration in brightness is damage in the fluorescent substance due to impact caused by ions generated at the time of plasma discharges.

❑ Practical value for Image sticking

The relationship between integrated lighting time and brightness in this plasma module is described in the attached material. In particular, the deterioration in brightness tends to be accelerated up to 100 hours in the initial period. In the initial period, the fixed display of patterns particularly tends to cause image sticking. The practical value for image sticking is difficult in concrete numerals. As described below, you are advised to take proper measures to make the occurrence of image sticking as slow as possible.

❑ Proposed measures taken to relieve image sticking

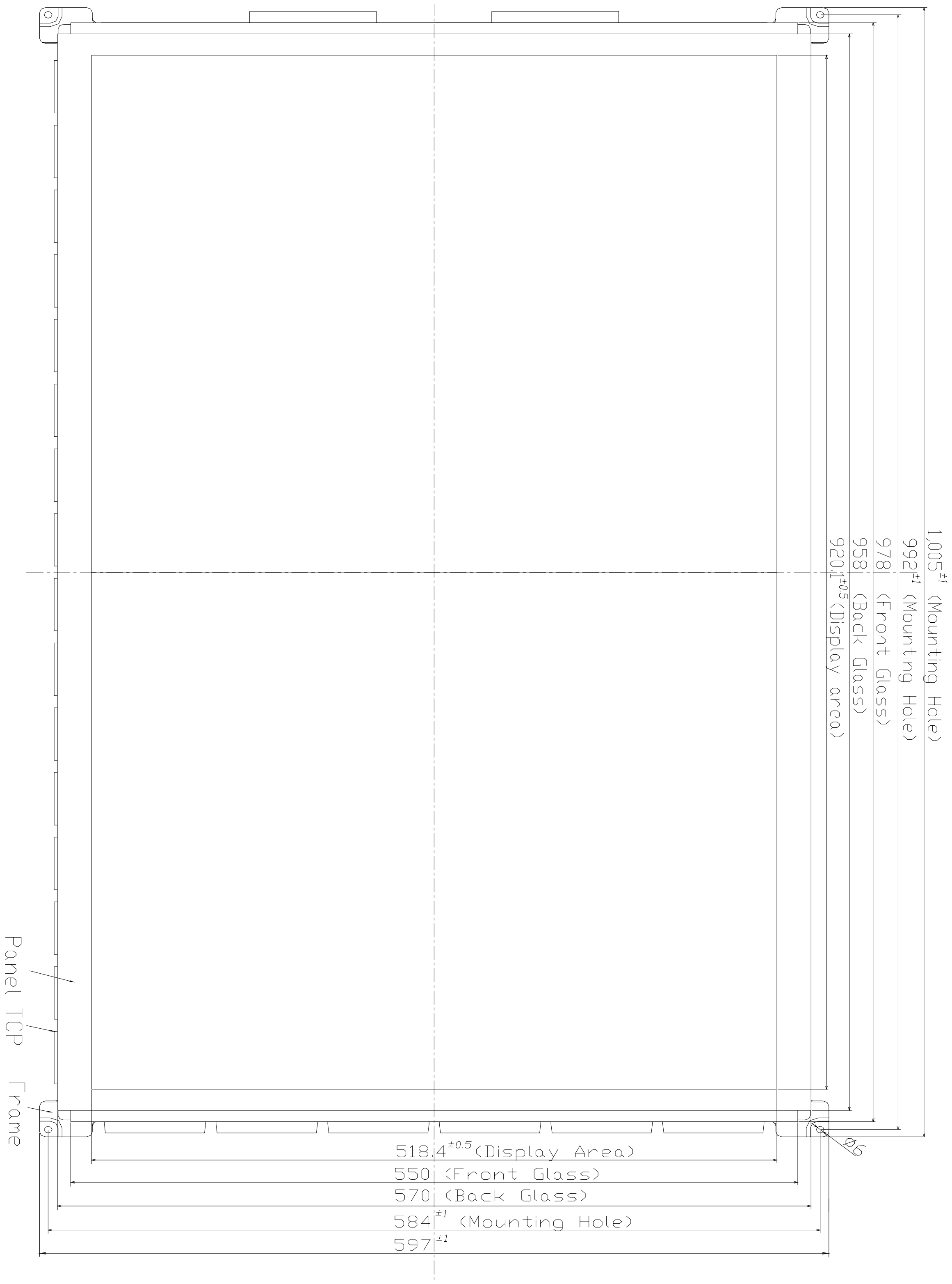
So long as there is the reduction of brightness in the fluorescent substance, it is impossible to avoid the occurrence of image sticking. Therefore, to relieve image sticking, we offer you a method of entering an image input that may ensure reluctance to the generation of the difference in brightness reduction among the displayed dots.
The images from TV broadcasting involve a high rate of motion picture displays. Therefore, there is less chance of being a cause of difference in brightness reduction among the cells. Even when the fixed patterns are displayed, they generally last for a few minutes. Since the same pattern is less liable to be displayed, there is almost no influence toward image sticking.

If the fixed patterns tend to be displayed for a long time, however, there occurs a substantial imbalance between the lighting and non-lighting areas, thus causing a difference in brightness as a result. In this document, we offer you some proposals of installation, paying attentions to the two points: the reduction of difference in brightness achieved by integrated lighting time leveling and the method of edge smearing to make image sticking hard to be discerned.
The result from these proposals can, however, greatly depend on the contents of images and the operating environment. Therefore, we consider that it is essential to take the suitable measures in consideration of the customer's operating environment.

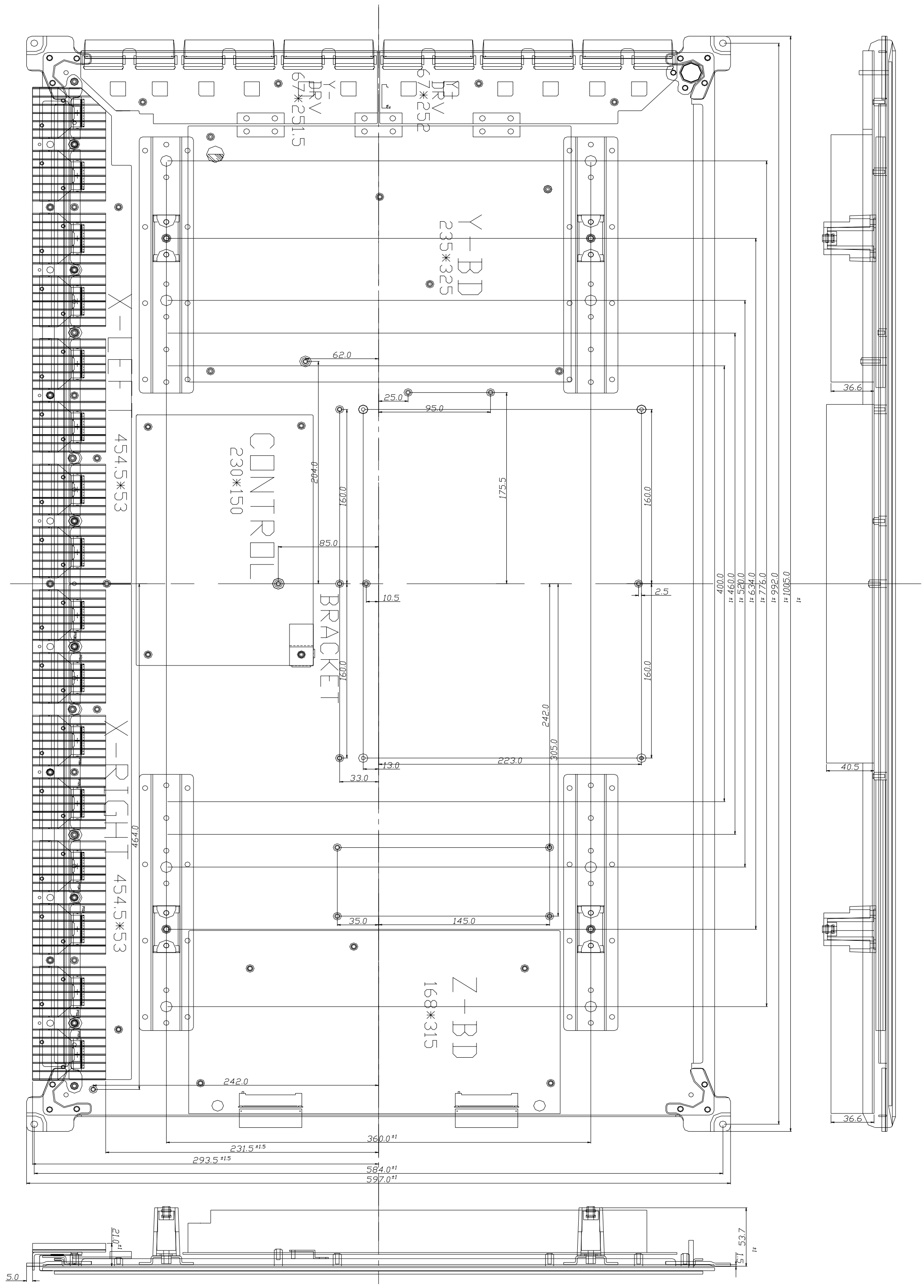
Example of Proposal 1: The display position is moved while the fixed display pattern is changed over, or it is scrolled during the display.
Example of Proposal 2: If possible, a pattern of complementary color is incorporated (for integrated time leveling).
Example of Proposal 3: The fixed pattern and the motion picture display are reciprocally exchanged, in order to minimize display period of the fixed pattern.
Example of Proposal 4: During operation, the brightness of screen is suppressed as low as possible.
For the display patterns, characters are indicated not on the black ground (non-picture area) but on the colored ground (mixture of R, G, B recommended).

6. OUTLINE DRAWING

❑ **Front View**



❑ Rear View


Y-BD
235*325
CONTROL
230*150
BRACKET
Z-BD
168*315
X-LEFT
454.5*53
X-RIGHT
454.5*53

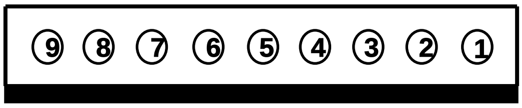
7. CONNECTORS and CONNECTIONS

❑ Power Input Connector

Connector P2002 Pin Assignment(Y SUS Board)

Pin No.	Symbol	Pin No.	Symbol
1	+5V	7	NC
2	GND	8	Vs
3	Va	9	Vs
4-6	GND		

1-1123723-9 Pin numbers
(view from the pin connection side)

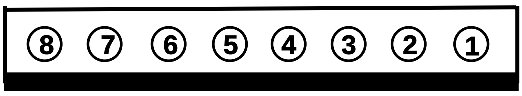


Module side connector : 1-1123723-9 (Header)
Mating Connector : 1-1123722-9 (Housing)
Connector Supplier : AMP

Connector P3001 Pin Assignment (Z SUS Board)

Pin No.	Symbol	Pin No.	Symbol
1	Vs	5	GND
2	Vs	6	Va
3	N.C	7	GND
4	GND	8	+5V

1-1123723-8 Pin numbers
(View from the pin connection side)

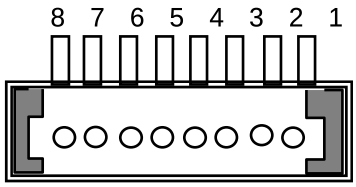


Module side connector : 1-1123723-8 (Header)
Mating Connector : 1-1123722-8 (Housing)
Connector Supplier : AMP

Connector P1300 Pin Assignment (Control Board)

Pin No.	Symbol	Pin No.	Symbol
1	+5V	5	GND
2	+5V	6	GND
3	+5V	7	GND
4	+5V	8	GND

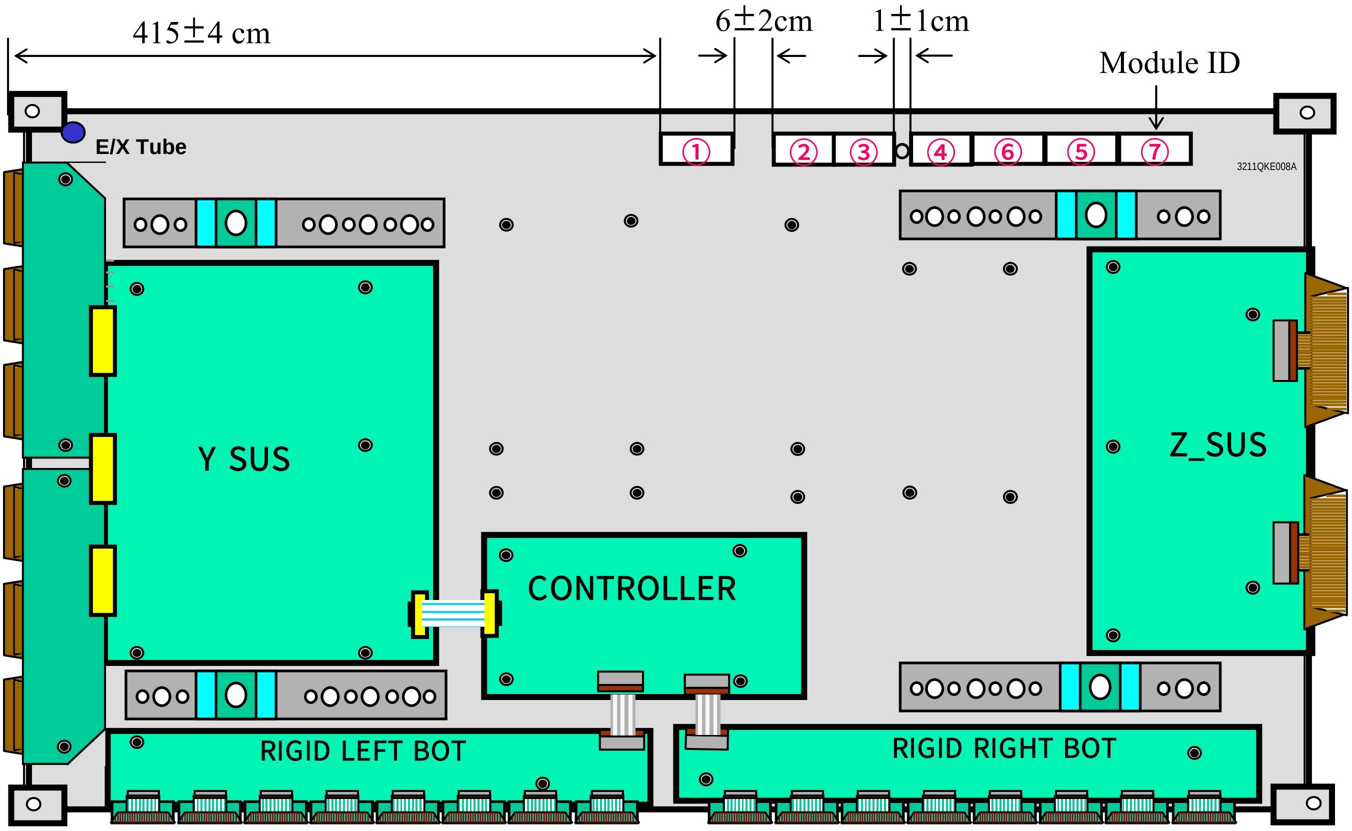
GT200-8P-SS-A Pin numbers
(View from the pin connection side)



Connector : GT200-8P-SS-A
Housing : GIL-S-8S-S2C2-S
Mkaer : LG Cable

8. LABEL

❑ LABEL Sticking Position



❑ LABEL ① : Identification Label



① Model Name
② Bar Code (Code 128, Contains the manufacture No.)
③ Manufacture No.
④ The trade name of LG Electronics
⑤ Manufactured date (Year & Month)
⑥ The place Origin
⑦ Model Suffix

❑ LABEL ② : Warning Label (High Voltage)



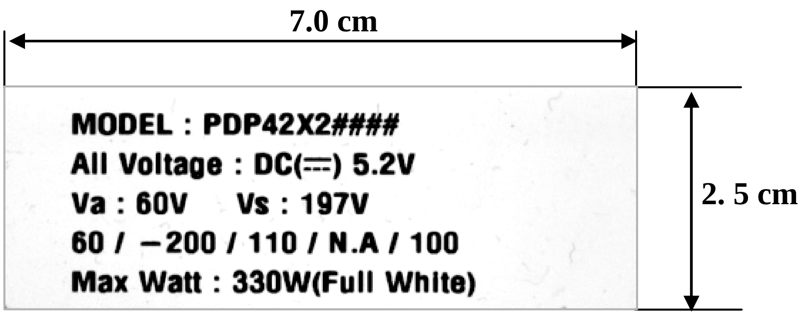
❑ LABEL ③ : Warning Label (Hot Surface)



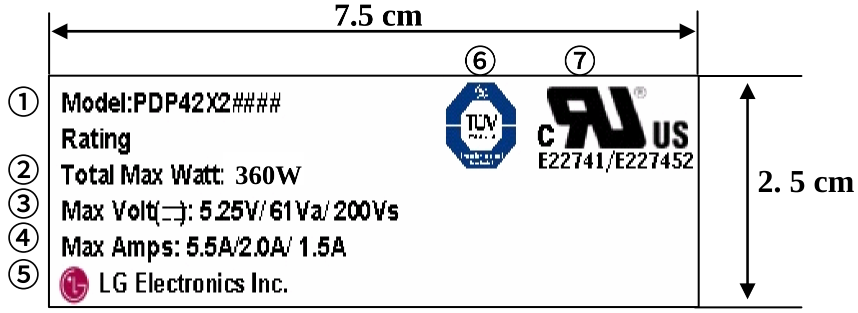
❑ LABEL ④ : Caution Label (Mechanical Hazard)



❑ LABEL ⑤ : Voltage Label (Model Name & Operational Voltage)



❑ LABEL ⑥ : Safety Approval Label



① Model Name
② Max. Watt
③ Max. Volts
④ Max. Amps
⑤ The Trade Name of LG Electronics
⑥ TUV Approval Mark
⑦ Safety Approval Mark
⑧ Safety Approval No.

9. PACKING

❑ Box packing (5 modules per each Box)

1. Prepare to Module & Packing sheet (Grid)
-Put the Module on the printed surface as four holes at the sheet locate to down of the module like the picture below.
-It has to use some supporter of 10cm height in the bottom of the module.

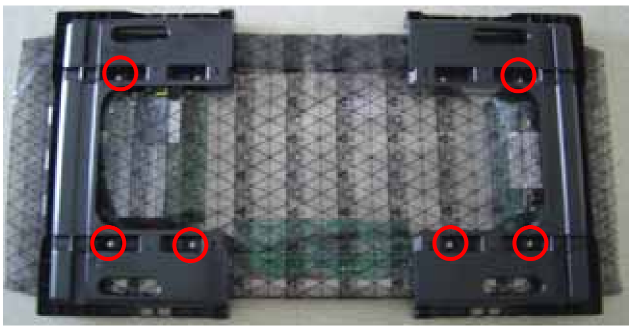


2. Wrapping Packing sheet
- Fold the packing sheet, align 4 holes of the sheet with support sides of the module and then tapping.
-Do not fold the right/left side of the sheet.

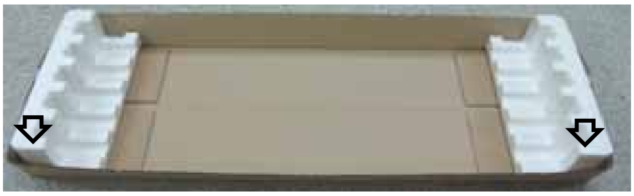


3. Connect Cover Plate
-Connect M4 screw(6 positions)
-Screw torque: 17~20kgf.cm
-The shape of Cover Plate is same (Top/Bottom, Right/Left)





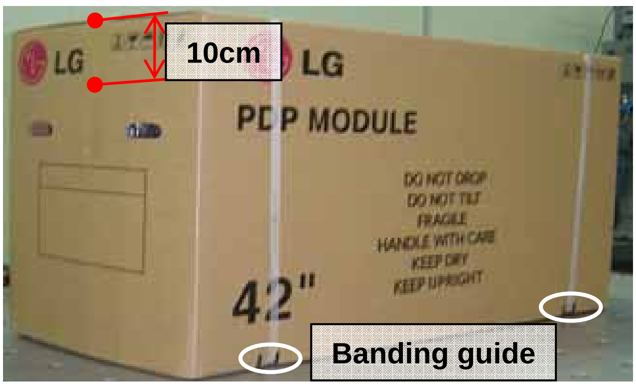
4. Prepare bottom Box for Packing
-The arrow direction at the bottom packing Should be front side.



5. Insert wrapped modules with top packings
-Insert wrapped modules arrow direction of the bottom packing in the bottom box.
-Top packings should be inserted front side like the picture below.

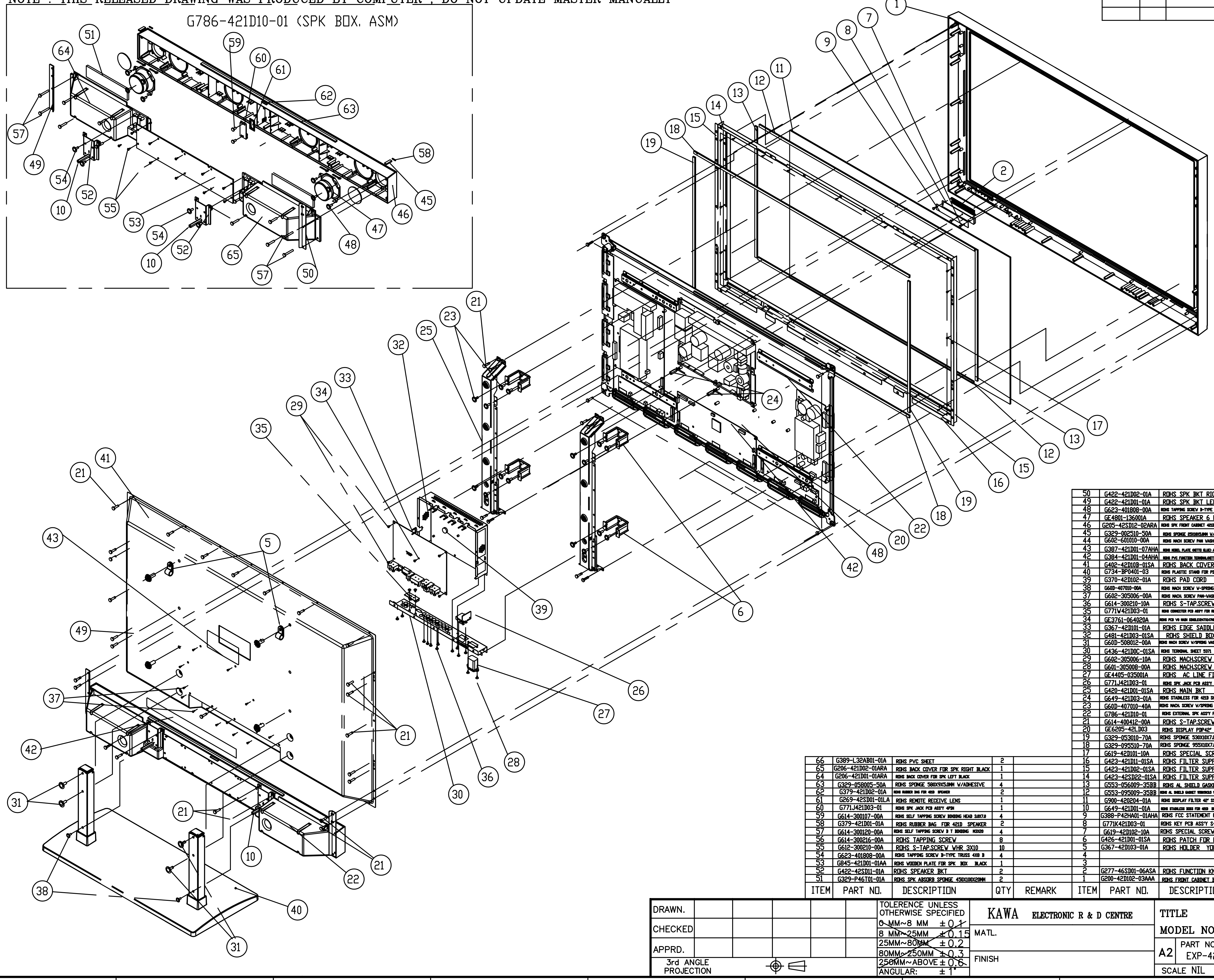


6. Put Box, Tapping and Banding
-Put Box on Module(the direction of Box should be same direction as front side of Module.
-Box Tapping should be down to 10cm at right/left side like picture as shown below.
- Box banding by using the location of Banding guide.



NOTE : THIS RELEASED DRAWING WAS PRODUCED BY COMPUTER , DO NOT UPDATE MASTER MANUALLY

DWG. REV.	ZONE	DESCRIPTION	DATE	REVISOR



ITEM	PART NO.	DESCRIPTION	QTY	REMARK
66	G389-L32AB01-01A	ROHS PVC SHEET	2	
65	G206-421D02-01ARA	ROHS BACK COVER FOR SPK RIGHT BLACK	1	
64	G206-421D01-01ARA	ROHS BACK COVER FOR SPK LEFT BLACK	1	
63	G329-058005-50A	ROHS SPONGE 580X9X5.0MM W/ADHESIVE	4	
62	G379-421D02-01A	ROHS RUBBER BAG FOR 421D SPEAKER	2	
61	G269-42SD01-01LA	ROHS REMOTE RECEIVE LENS	1	
60	G771J421D03-01	ROHS SPK JACK PCB ASS'Y 4PIN	1	
59	G614-300107-00A	ROHS SELF TAPPING SCREW BINDING HEAD 3.0X7.0	4	
58	G379-421D01-01A	ROHS RUBBER BAG FOR 421D SPEAKER	2	
57	G614-300120-00A	ROHS SELF TAPPING SCREW B T BINDING M3X20	4	
56	G614-300216-00A	ROHS TAPPING SCREW	8	
55	G612-300210-00A	ROHS S-TAP.SCREW WHR 3X10	10	
54	G623-401808-00A	ROHS TAPPING SCREW B-TYPE TRUSS 4X8 B	4	
53	G845-421D01-01AA	ROHS WOODEN PLATE FOR SPK BOX BLACK	1	
52	G422-42SD11-01A	ROHS SPEAKER BKT	2	
51	G329-P46T01-01A	ROHS SPK ABSORB SPONGE 450X100X20MM	2	

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
50	G422-421D02-01A	ROHS SPK BKT RIGHT	1	
49	G422-421D01-01A	ROHS SPK BKT LEFT	1	
48	G623-401808-00A	ROHS TAPPING SCREW B-TYPE TRUSS 4X8	16	
47	GE4801-136001A	ROHS SPEAKER 6 OHM 12W D3"	2	
46	G205-42SD12-02ARA	ROHS SPK FRONT CABINET 421D W/HOLE BLACK	1	
45	G329-002510-50A	ROHS SPONGE 25X10X5.0MM W/ADHESIVE	1	
44	G602-601010-00A	ROHS MACH SCREW PAN WASHER M6.0X1.0PX10MM	6	
43	G387-421D01-07AHA	ROHS MODEL PLATE (GETTO GLUE) AKAI PDP4225TA	1	
42	G384-421D01-04AHA	ROHS PVC FUNCTION TERMINAL(GETTO GLUE) 421D	1	
41	G402-42D10B-01SA	ROHS BACK COVER 42HMD BLACK	1	
40	G734-BP0401-03	ROHS PLASTIC STAND FOR PDP421D CD=460MM	1	ASM
39	G370-42D102-01A	ROHS PAD CORD	1	
38	G60D-407010-00A	ROHS MACH SCREW W-SPRING WASHER M4X10	2	
37	G602-305006-00A	ROHS MACH. SCREW PAN-WASHER 3X6	16	
36	G614-300210-10A	ROHS S-TAP.SCREW BID 3X10	9	
35	G771W421D03-01	ROHS CONNECTER PCB ASS'Y FOR REMOTE S-MT5371	1	ASM
34	GE3761-064020A	ROHS PCB V0 MAIN SINGLE(247X147MM) 1IN(247X152MM) 2 HDMI	1	
33	G367-42D101-01A	ROHS EDGE SADDLE 14MM 42D1	5	
32	G481-421D03-01SA	ROHS SHIELD BOX 5371	1	
31	G60D-508012-00A	ROHS MACH SCREW W/SPRING WASHER M5X0.8X12MM BZP	4	
30	G436-421D0C-01SA	ROHS TERMINAL SHEET 5371	1	
29	G602-305006-10A	ROHS MACH.SCREW WHR 3X6	8	
28	G601-305008-00A	ROHS MACH.SCREW CTS 3X8	2	
27	GE4405-035001A	ROHS AC LINE FILTER	1	
26	G771J421D03-01	ROHS SPK JACK PCB ASS'Y 4PIN S-MT5371	1	
25	G420-421D01-01SA	ROHS MAIN BKT 421D	2	
24	G649-421D03-01A	ROHS STAINLESS FOR 421D SHIELD BOX H=19.5MM	2	
23	G60D-407010-40A	ROHS MACH. SCREW W/SPRING WASHER M4.0X0.7X10MM	16	
22	G786-421D10-01	ROHS EXTERNAL SPK ASS'Y FOR W/WINDOW BLACK	1	ASM
21	G614-400412-00A	ROHS S-TAP.SCREW BID 4X12	44	
20	GE6205-42LD03	ROHS DISPLAY PDP42" LG-42X3/X3A	1	
19	G329-053010-70A	ROHS SPONGE 530X10X7.0MM W/ADHESIVE	2	
18	G329-095510-70A	ROHS SPONGE 955X10X7.0MM W/ADHESIVE	2	
17	G619-42D101-10A	ROHS SPECIAL SCREW 3X10	24	
16	G423-421D11-01SA	ROHS FILTER SUPPORT BOTTOM	1	
15	G423-421D02-01SA	ROHS FILTER SUPPORT L&R	2	
14	G423-42SD22-01SA	ROHS FILTER SUPPORT TOP	1	
13	G553-056009-35BB	ROHS AL SHIELD GASKET 560X9X3.5	2	
12	G553-095009-35BB	ROHS AL SHIELD GASKET 950X9X3.5 W/CONDUCTIVE ADHESIVE	2	
11	G900-420204-01A	ROHS DISPLAY FILTER 42" SSC FOR LG 972X560X3.2	1	
10	G649-421D01-01A	ROHS STAINLESS BOSS FOR 421D SPEAKER H45	2	
9	G388-P42HA01-01AHA	ROHS FCC STATEMENT PLATE 77X20MM	1	
8	G771K421D03-01	ROHS KEY PCB ASS'Y S-MT5371 FOR PDP421D	1	
7	G619-42D102-10A	ROHS SPECIAL SCREW 2.6X6 NP '+'	3	
6	G426-421D01-01SA	ROHS PATCH FOR LGE 421D	4	
5	G367-42D103-01A	ROHS HOLDER YONG RONG	2	
4				
3				
2	G277-46SD01-06ASA	ROHS FUNCTION KNOB BLACK	1	
1	G200-42D102-03AAA	ROHS FRONT CABINET BLACK AKAI	1	

DRAWN.				TOLERENCE UNLESS OTHERWISE SPECIFIED	KAWA ELECTRONIC R & D CENTRE	TITLE GPDP421DAIA1LS-B02
CHECKED				0 MM~8 MM ±0.1 8 MM~25MM ±0.15	MATL.	MODEL NO.
APPRD.				25MM~80MM ±0.2 80MM~250MM ±0.3	FINISH	A2 PART NO. EXP-421D08-01 / DWG. NO. 421DEXP8
3rd ANGLE PROJECTION				250MM~ABOVE ±0.6 ANGULAR: ±1°		SCALE NIL / QTY. / SHEET 1 OF 1

Spare part list for PDP42Z5TAC

Item	Part Number	Part Description	Usage / unit	Unit	Key/Spare
1>	GPDP421DAIA1LS-B02	ROHS AKAI PDP421D (PDP42Z5TAC) S-MT5371 LGX3A AC120V/60HZ CANADA BLACK HORZONTAL DTV			
	G510-421D02-03ALA	ROHS CARTON BOX AKAI PDP42Z5TAC(S-MT5371) LGX3 CANADA L ZHEN XING	1.000000	Piece	K
2>	G580-421D4C-01APA	ROHS IB E FOR AKAI PDP42Z5TAC TV +DTV+V-CHIP NO PIP LGX3A MT5371 CANADA(CHENG YI)	1.000000	Piece	K
3>	G580-K00201-01CPA	ROHS IB E FOR AKAI W/O DVD K002 (OMNIPOTENCE) REMOTE CONTROL USA ADD SAFETY(CHENG YI)	1.000000	Piece	K
4>	G580@K00201-04BPA	ROHS IB FR FOR AKAI K002 (OMNIPOTENCE) REMOTE CONTROL USA "F2" TO "GUIDE" ADD SAFETY	1.000000	Piece	K
5>	GE7501-063009-1A	ROHS REMOTE CONTROC K002 231 MASK "AKAI"64KEYS BLACK (COMMON) OMNIPOTENCE(CHUAN QI SHENG)	1.000000	SET	K
6>	G771E421D04-01	ROHS MAIN PCB ASS'Y S-MT5371	1.000000	SET	K
7>	G200-42D102-03AAA	ROHS FRONT CABINET 421D(B) BLACK (P320-605871K-00) AKAI A(AKAI PLASTIC)	1.000000	Piece	S
8>	G277-46SD01-06ASA	ROHS FUNCTION KNOB BLACK(P320-605871K-00) S(AKAI PLASTIC)	1.000000	Piece	S
9>	G300-421D03-07NA	ROHS POLYFOAM BOTTOM FOR 421D HORIZONTAL PACKING LAN DO WANG	1.000000	Piece	S
10>	G300-421D04-07NA	ROHS POLYFOAM TOP FOR 421D HORIZONTAL PACKING LAN DO WANG	1.000000	Piece	S
11>	G300-421D05-01NA	ROHS POLYFOAM LEFT SIDE 421D HORIZONTAL PACKING LAN DO WANG	1.000000	Piece	S
12>	G300-421D06-01NA	ROHS POLYFOAM RIGHT SIDE FOR 421D HORIZONTAL PACKING	1.000000	Piece	S
13>	G310-111404-07VA	ROHS POLYBAG 11"X14"X0.04 FV (AO LANG)	1.000000	Piece	S
14>	G310-421D01-01TA	ROHS POLYBAG W/NUTI LANGUAGE WARNING&RECYCLE&HOLE (FOR 421D HORIZOTAL) PENG KUN	1.000000	Piece	S
15>	G329-053010-70A	ROHS SPONGE 530X10X7.0MM W/ ADHESIVE	2.000000	Piece	S
16>	G329-095510-70A	ROHS SPONGE 955X10X7.0MM W/ ADHESIVE	2.000000	Piece	S
17>	G361-150208-01A	ROHS CABINET TIE 150X2.0X0.8MM AO LANG	2.000000	Piece	S
18>	G367-42D103-01A	ROHS HOLDER YONG RONG	2.000000	Piece	S

19>	G384-421D01-04AHA	ROHS PVC FUNCTION TERMINAL (NITTO.GLUE) 421D(S-MT5371) W/SPK TER H jia li	1.000000	Piece	S
20>	G387-421D01-08AHA	ROHS MODEL PLATE(NITTO GLUE) AKAI PDP42Z5TAC(S-MT5371) LGX3 CANADA H JIA LI	1.000000	Piece	S
21>	G388-42D103-01HA	ROHS CAUTION PLATE ENG 42D1 H (JIA LI)	1.000000	Piece	S
22>	G388-42SD01-01A	ROHS PC SHEET FOR KEY PCB (JIA LI)	1.000000	Piece	S
23>	G388-P42HA01-01AHA	ROHS FCC STATEMENT PLATE 77X20MM H JIA LI	1.000000	Piece	S
24>	G402-42D10B-01SA	ROHS BACK COVER 42HMD BLACK S (JIE QI)	1.000000	Piece	S
25>	G426-421D01-01SA	ROHS PATCH FOR LGE 421D(TOMEI)	4.000000	Piece	S
26>	G436-421D0C-01SA	ROHS TERMINAL SHEET 5371(TOMEI)	1.000000	Piece	S
27>	G481-421D03-01SA	ROHS SHIELD BOX 5371(TOMEI)	1.000000	Piece	S
28>	G512-421D0B-01A	ROHS PROTECT CONER FOR 421D HORIZONTAL PACKING LAN DO WANG	2.000000	Piece	S
29>	G553-002007-25BB	ROHS AL SHIELD GASKET 20X7X2.5MM W/CONDUCTIVE ADHESIVE(SHI KE FA)	6.000000	Piece	S
30>	G553-005007-10BB	ROHS AL SHIELD GASKET 50X7X1.0MM W/CONDUCTIVE ADHESIVE(SHI KE FA)	1.000000	Piece	S
31>	G553-006007-25BB	ROHS AL SHIELD GASKET 60X7X2.5MM W/CONDUCTIVE ADHESIVE(SHI KE FA)	4.000000	Piece	S
32>	G553-007007-10BA	ROHS AL SHIELD GASKET 70X7X1.0 W/ CONDUCTIVE ADHESIVE	4.000000	Piece	S
33>	G553-007007-10BB	ROHS AL SHIELD GASKET 70X7X1.0 W/ CONDUCTIVE ADHESIVE(SHI KE FA)	1.000000	Piece	S
34>	G553-008007-10BA	ROHS AL SHIELD GASKET 80X7X1.0 W/ CONDUCTIVE ADHESIVE	8.000000	Piece	S
35>	G553-009507-10BA	ROHS AL SHIELD GASKET 95X7X1.0 W/ CONDUCTIVE ADHESIVE	2.000000	Piece	S
36>	G553-009507-10BB	ROHS AL SHIELD GASKET 95X7X1.0 W/ CONDUCTIVE ADHESIVE(SHI KE FA)	1.000000	Piece	S
37>	G553-011007-25BB	ROHS AL SHIELD GASKET 110X7X2.5MM W/CONDUCTIVE ADHESIVE(SHI KE FA)	4.000000	Piece	S

Spare part list for PDP42Z5TAC

38>	G553-012507-25BB	ROHS AL SHIELD GASKET 125X7X2.5MM W/CONDUCTIVE ADHESIVE(SHI KE FA)	8.000000	Piece	S
39>	G553-013507-10BB	ROHS AL SHIELD GASKET 135X7X1.0 W/CONDUCTIVE ADHESIVE(SHI KE FA)	1.000000	Piece	S
40>	G553-020007-25BB	ROHS AL SHIELD GASKET 200X7X2.5MM W/CONDUCTIVE ADHESIVE(SHI KE FA)	4.000000	Piece	S
41>	G553-056009-35BB	ROHS AL SHIELD GASKET 560X9X3.5 W/CONDUCTIVE ADHESIVE(SHI KE FA)	2.000000	Piece	S
42>	G553-095009-35BB	ROHS AL SHIELD GASKET 950X9X3.5 W/CONDUCTIVE ADHESIVE(SHI KE FA)	2.000000	Piece	S
43>	G554-030030-01BB	ROHS AL SHIELD PLATE 30X30MM W/ CONDUCTIVE ADHESIVE	1.000000	Piece	S
44>	G563-119-A	ROHS SERIAL NO. LABEL	1.000000	Piece	S
45>	G568-P46T02-02A	ROHS WARNING LB ENG 42SF NIL	1.000000	Piece	S
46>	G579-421D01-11APA	ROHS BAR CODE LABEL (W/SERIAL NO) PDP42Z5TAC CANADA P(QIAN SE)	2.000000	Piece	S
47>	G579-42D102-09A	ROHS SERIAL NO/BAR CODE LABEL 42D1	1.000000	Piece	S
48>	G579-42D105-01A	ROHS PROTECTIVE EARTH LABEL FOR ESA 42TD1	1.000000	Piece	S
49>	G579@421D04-03APA	ROHS BOX LABEL AKAI FRENCH PDP42Z5TAC CANADA P	1.000000	Piece	S
50>	G590-421D01-12APA	ROHS WARRANTY CARD AKAI ENG PDP42Z5TAC(CANADA) P(QIAN SE)	1.000000	Piece	S
51>	G590@421D01-13APA	ROHS WARRANTY CARD AKAI FRENCH PDP42Z5TAC CANADA P	1.000000	Piece	S
52>	G593-421D01-16APA	ROHS QSG CARD ENG PDP42Z5TAC (S-MT5371) CANADA P(QIAN SE)	1.000000	Piece	S
53>	G900-420204-01A	ROHS DISPLAY FILTER 42" SSC FOR LG 972X560X3.2 (L6-COATING TYPE)	1.000000	Piece	S
54>	GE3404-157004A	ROHS AC CORD UL 1.88M (YY-3/ST3 YUNBIAO) (YUN HUAN)	1.000000	Piece	S
55>	GE3421-925268A	ROHS WIRE ASSY 1H2.5-2H2.5 AG L300/250 8+12/4+7+2+12P 42PDP MT5371 (HU GUANG)	1.000000	Piece	S
56>	GE3421-926177A	ROHS WIRE ASSY 1H2.5-2H2.5 L360 AG 4/3+3P PDP42 MT5371 SPK (HU GUANG)	1.000000	Piece	S

Spare part list for PDP42Z5TAC

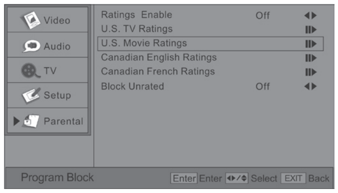
57>	GE3471-000134A	ROHS WIRE ASSY 1H2.0-2H2.0 L400/100 DI 13/9+5P PDP42 MT5371 KEY EMI (HU GUANG)	1.000000	Piece	S
58>	GE3471-004005A	ROHS WIRE WS SHIELD ASSY LVDS P1.25 30P/31P L=300 FOR 42LGX3 MT8202 W/EMI (PCB-4) (HU GUANG)	1.000000	Piece	S
59>	GE3701-058040A	ROHS PCB VO 50X19 REMOTE CONNECTER MT8202 COSTDOWN (LUEN SENG)	1.000000	Piece	S
60>	GE6205-42LD03	ROHS DISPLAY PDP42" LG-42X3(XGA)	1.000000	Piece	S
61>	GE7301-010002A	ROHS BATTERY AAA R03P1.5V <2> (CHAO YANG)	2.000000	Piece	S
62>	G734-BP0401-03	ROHS PLASTIC STAND FOR PDP421D CD=460MM W/O PACKING BLACK (605870)	1.000000	SET	S
63>	G771B421D03-01	ROHS IR RECEIVE PCB ASS'Y S-MT5371 FOR PDP42"	.000000	SET	S
64>	G771J421D03-01	ROHS SPK JACK PCB ASS'Y 4PIN S-MT5371	1.000000	SET	S
65>	G771K421D03-01	ROHS KEY PCB ASS'Y S-MT5371 FOR PDP421D	1.000000	SET	S
66>	G786-421D10-01	ROHS EXTERNAL SPK ASS'Y FOR W/ WINDOW BLACK(605870K) 6 OHM 12W S-MT5371	1.000000	SET	S

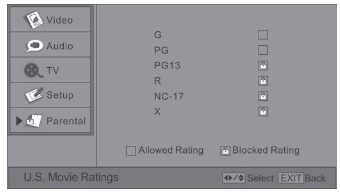
◆ Using the “U.S. Movie Ratings” item

① After entering the “Program Block” menu, press ∧ or ∨ button to highlight the “U.S. Movie Ratings” item.

② Press > or **Enter** button to enter.

③ Press ∧ or ∨ button to select an item, then press the **Enter** button to lock (display “🔒”) or unlock (display “☐ ”).





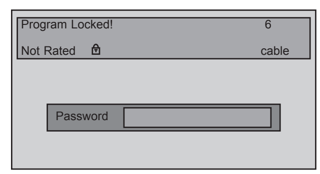
For Movie previously shown in theaters:

- G (general audience)
- PG (parental guidance suggested)
- PG-13 (13 years and older)
- R (Restricted)
- NC-17 (18 years and older)
- X (Adult)

If you set PG-13: G and PG movies be available, PG-13, R, NC-17, and X will be blocked.

④ Press the **Menu** button to exit the sub-menu.

◉ Unlocking programs temporarily



① If you try to watch a program that exceeds the TV Guideline you set, the system enters program lock mode. You can either unlock the program temporarily or select a non-locked program to watch.

② To temporarily unlock the program, press the Number buttons (0~9) to enter your 4-digit password.

If the correct code is entered, the program lock mode is released and the normal picture appears.

Software Upgrade

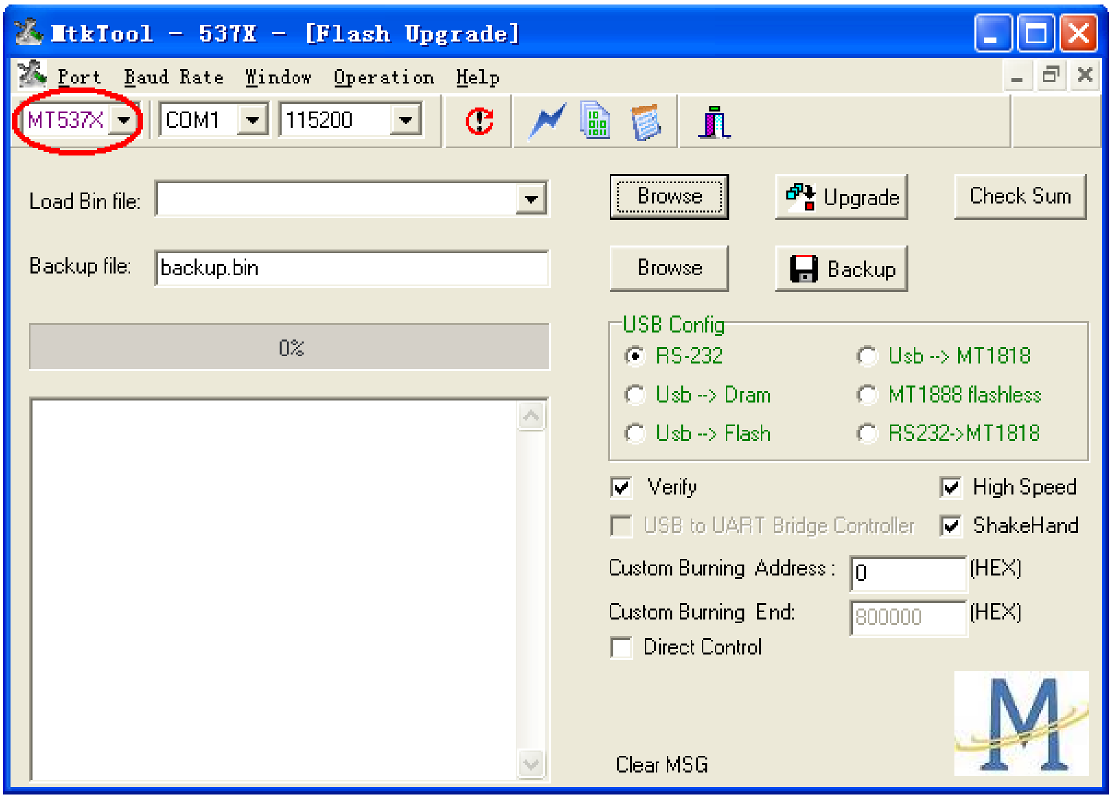
Process of update MT537X

Preparing :

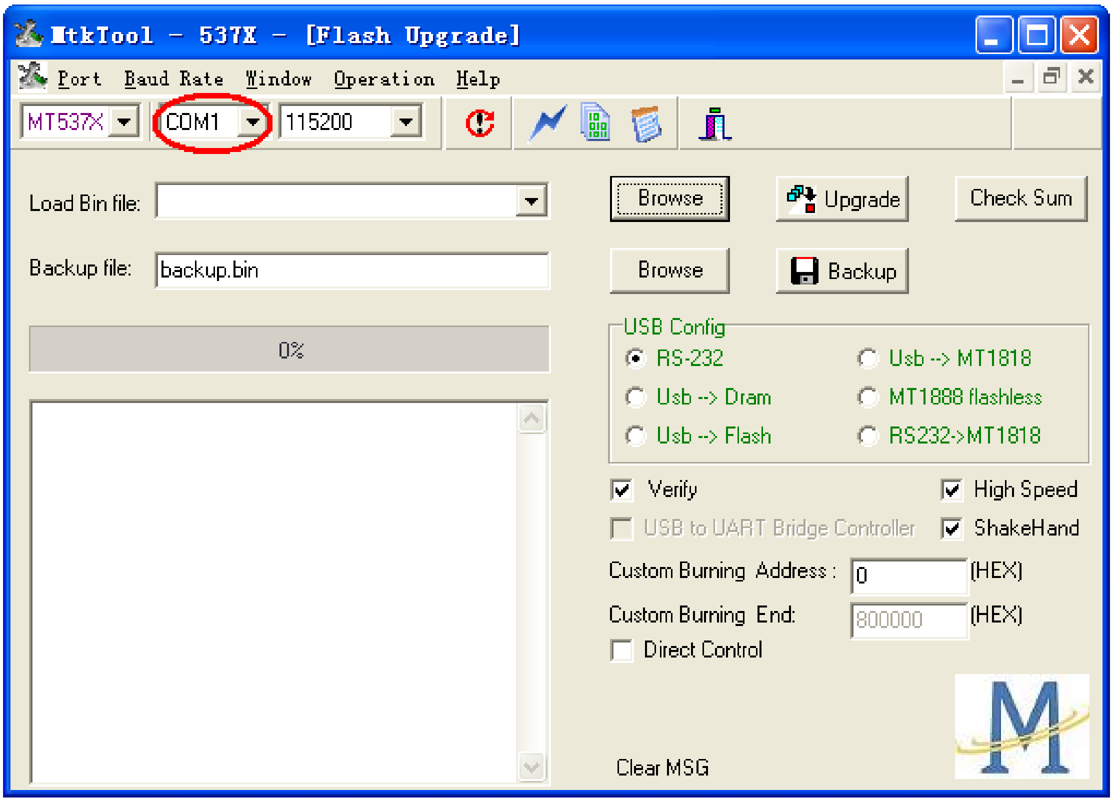
1. Connect the Plasma/LCD TV and PC with the **Software Upgrade Board**.Please find the details for connecting **refering to the appendix at the end of this file.**
2. Store the MtkTool into the PC .

Downloading :

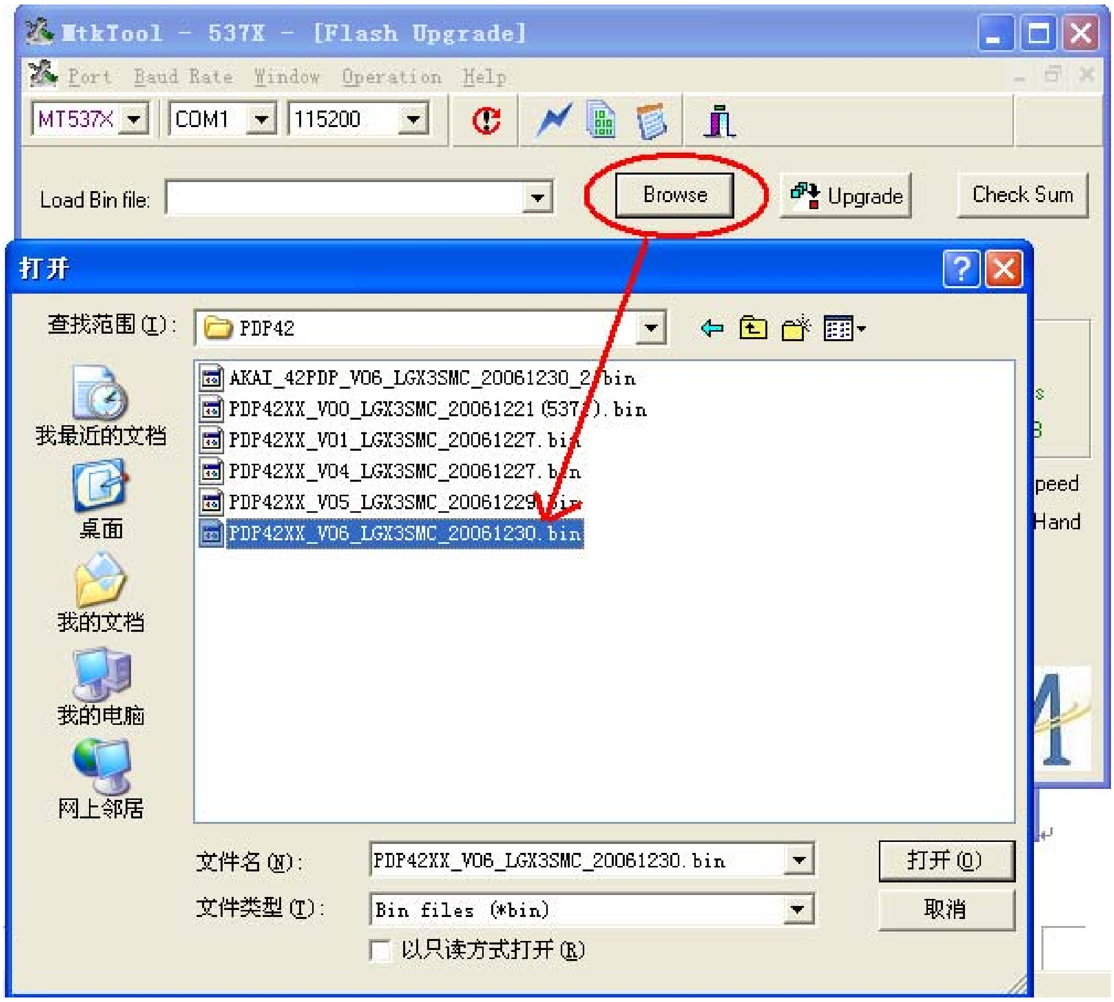
3. Turn on AC power of the TV and then press the button "standby" of the remote control . The image could be found on the screen of the TV while the color of the power indicator is green .
4. Execute MTKtool and select the chipset as MT537X. (the software of MTKtool will be sent to your side)



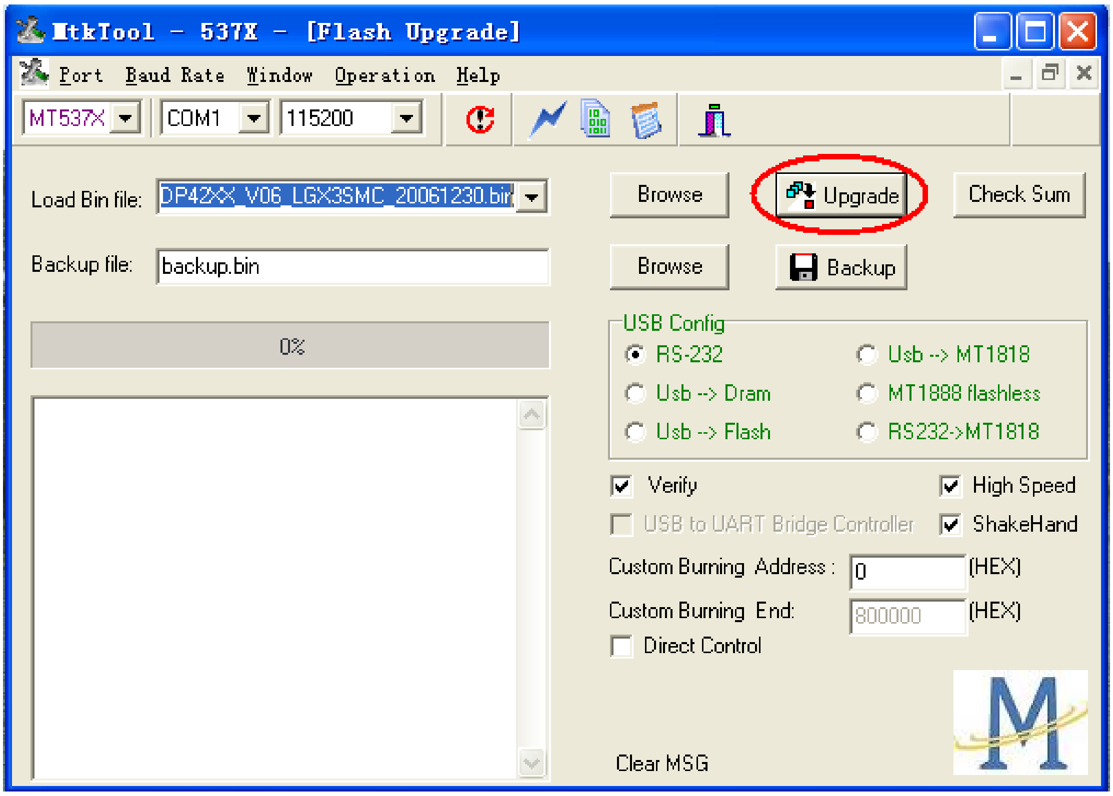
5. Select current COM port. (please try to check the COM port of your PC).

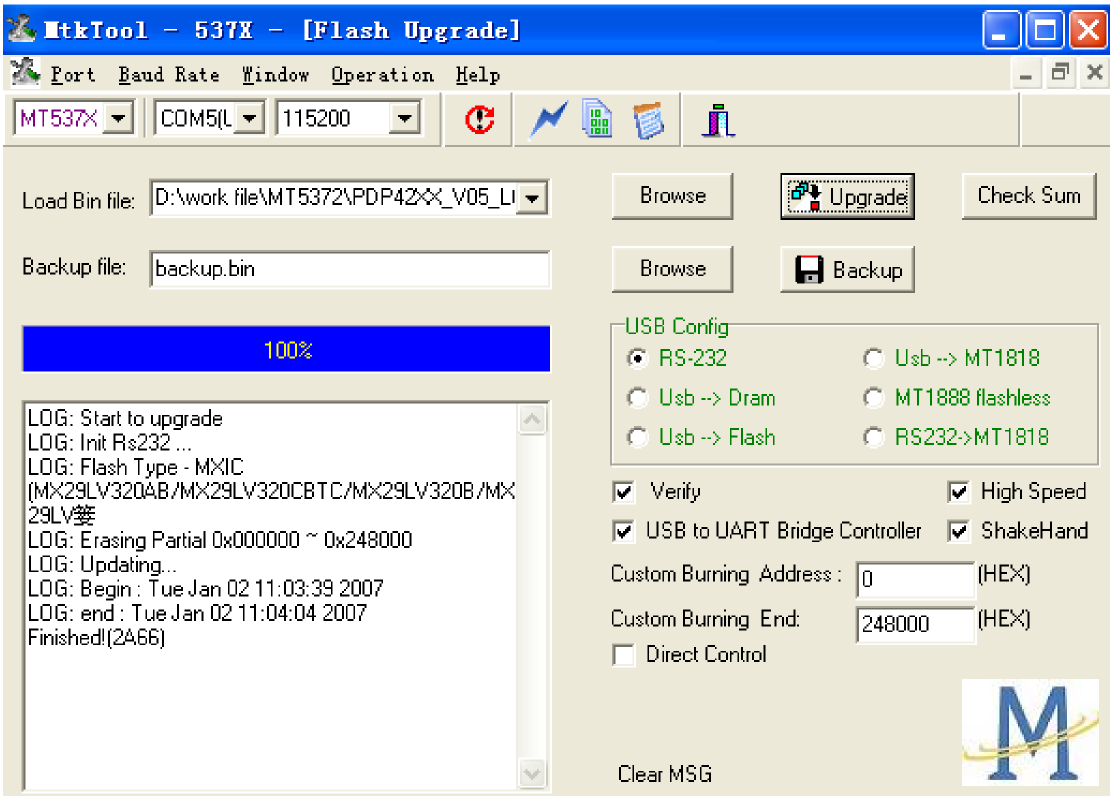


6. Choose the bit rate as 115200.
7. Select the update binary by pressing browse button. For example,the binary file name is PDP42XX_V06_LGX3SMC_20061230.bin. (this update firmware will be sent to your side)



8. Press Upgrade button and start update process.





9. The update process is successful as the progress bar is 100%. After the update process is ok, turn off power and wait indicator light is off. Turn on power and TV can work.

Checking

It is needed to check the version of the firmware for MT5371 which has been download into the TV .

Press Menu button of the remote control，following input “5371” of the remote control and OSD menu for Factory Setting is appeared on the screen .

Use the remote control and select the item of “Version Info” and then press “Enter” button of the remote control. It is easy to be found the version of the current firmware for MT5371 is as the following : “Model Name : PDP42Z5TA
/ Version:V17_LGX3SMC_20070119 ”

Appendix:

Quick Installation Guide

For

Software Upgrade Board

1. Parts List

- Software upgrade board x 1 (#1)
- RS232 null cable x 1 for PC (#2)
- RS232 – VGA cable (#4)
- USB cable x 1 (#5)

2. Installation for ATV upgrade

2.1 Connect RS232 cable (#2) to PC serial port



Connect another side of RS232 cable (#2) to the board (#1)



2.2 Connect RS232-VGA cable (#4) (RS232 side) to the board (#1)



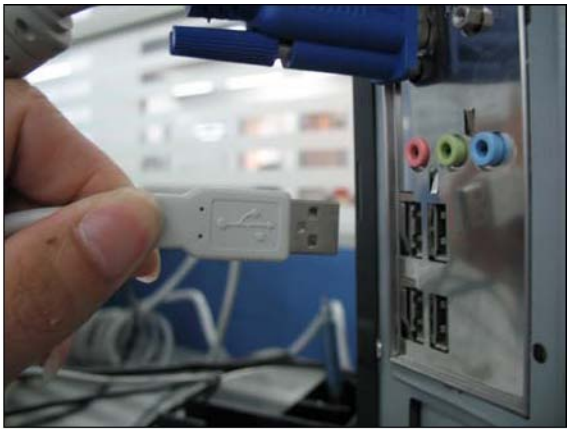
Connect RS232-VGA cable (#4) (VGA side) to the TV



2.3 Connect USB cable (#5) to the board (#1)

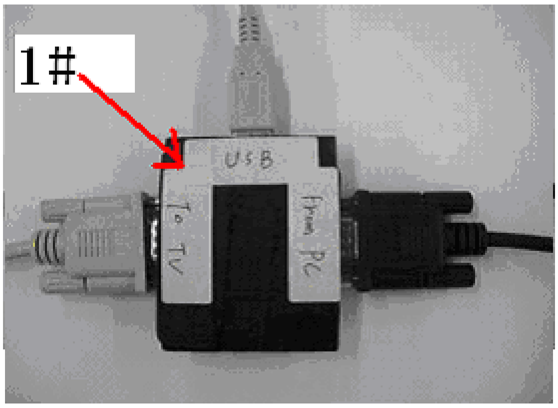


Connect another side of USB cable (#5) to PC

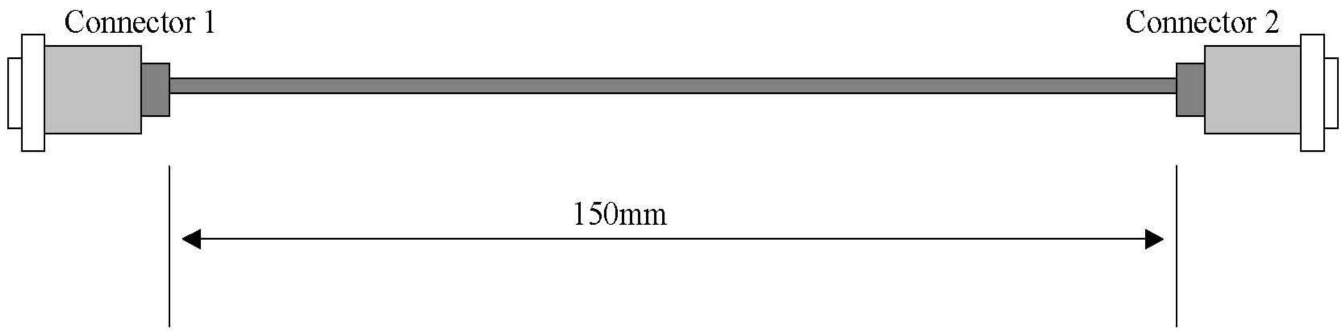


3. Cables Standard for Upgrade Board

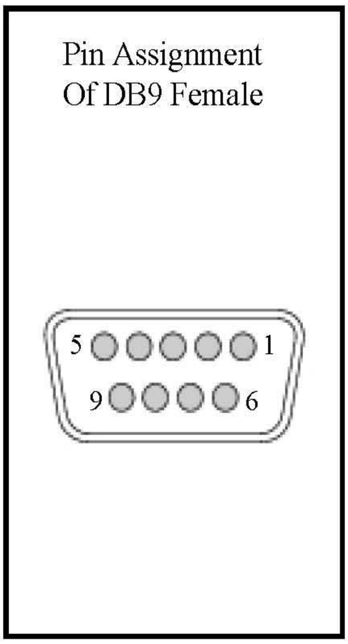
Software upgrade board x 1 (#1)

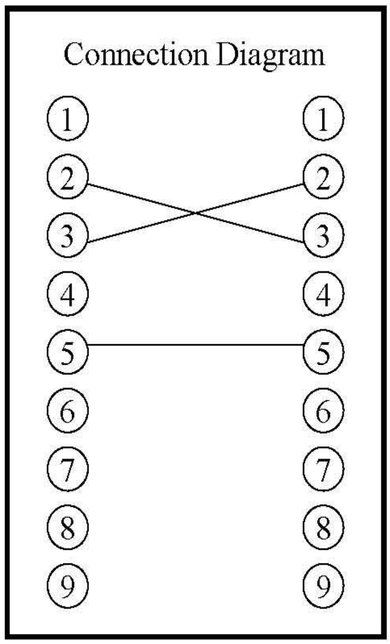


RS232 Null Cable for PC (#2)

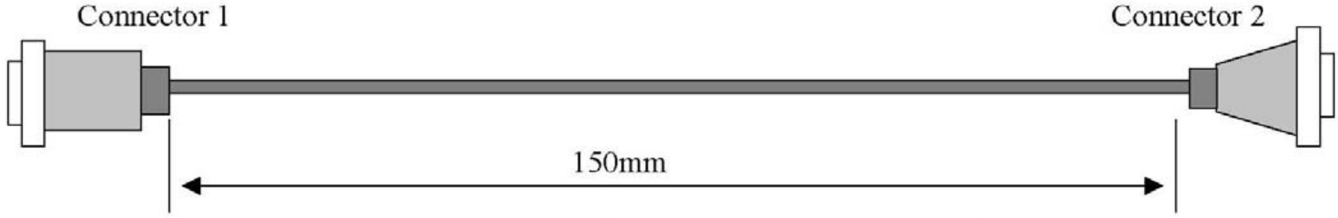


Connector 1: DB9 Female
Connector 2: DB9 Female

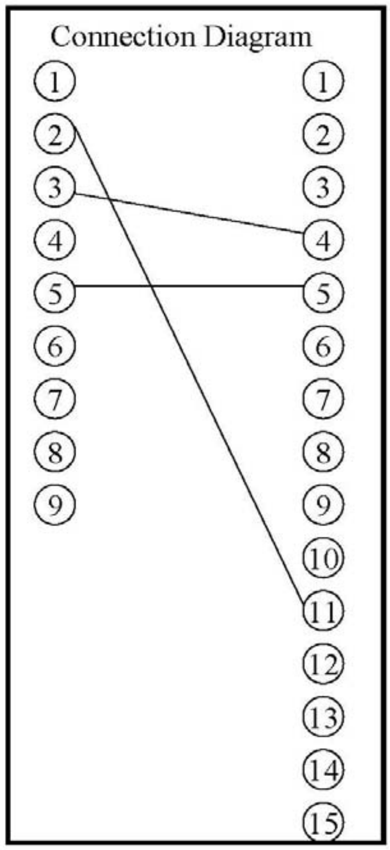




RS232 - VGA Cable (#4)

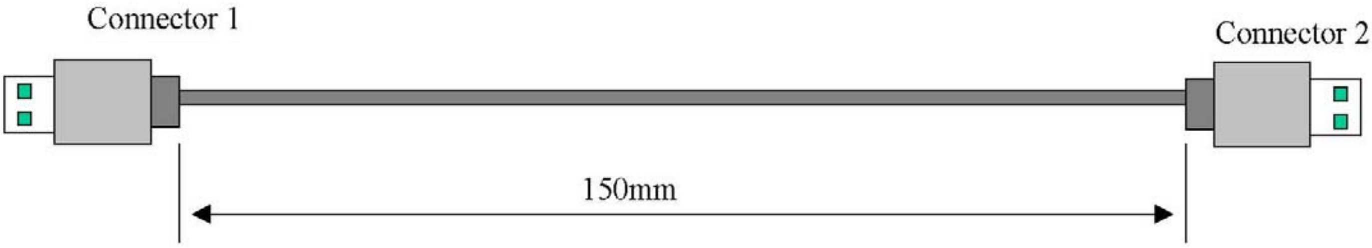






Connector 1: DB9 Female
Connector 2: VGA Male

USB Cable (#5)



Connector 1: Standard USB Male
Connector 2: Standard USB Male